Errata

Title & Document Type: 16550A State/Timing Logic Analyzer Service Guide

Manual Part Number: 16550-90901

Revision Date: April 1992

HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. The HP XXXX referred to in this document is now the Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

About this Manual

We've added this manual to the Agilent website in an effort to help you support your product. This manual provides the best information we could find. It may be incomplete or contain dated information, and the scan quality may not be ideal. If we find a better copy in the future, we will add it to the Agilent website.

Support for Your Product

Agilent no longer sells or supports this product. You will find any other available product information on the Agilent Test & Measurement website:

www.tm.agilent.com

Search for the model number of this product, and the resulting product page will guide you to any available information. Our service centers may be able to perform calibration if no repair parts are needed, but no other support from Agilent is available.

Agilent Technologies

Service Guide

Publication number 16550-90901
First edition, April 1992

HP 16550A
100-MHz State/500-MHz Timing Logic Analyzer

HP 16550A
100-MHz State/500-MHz Timing
Logic Analyzer

The HP 16550A is a 100-MHz State/500-MHz Timing Logic Analyzer module for the HP 16500A Logic Analysis System. The HP 16550A offers high performance measurement capability.

Features

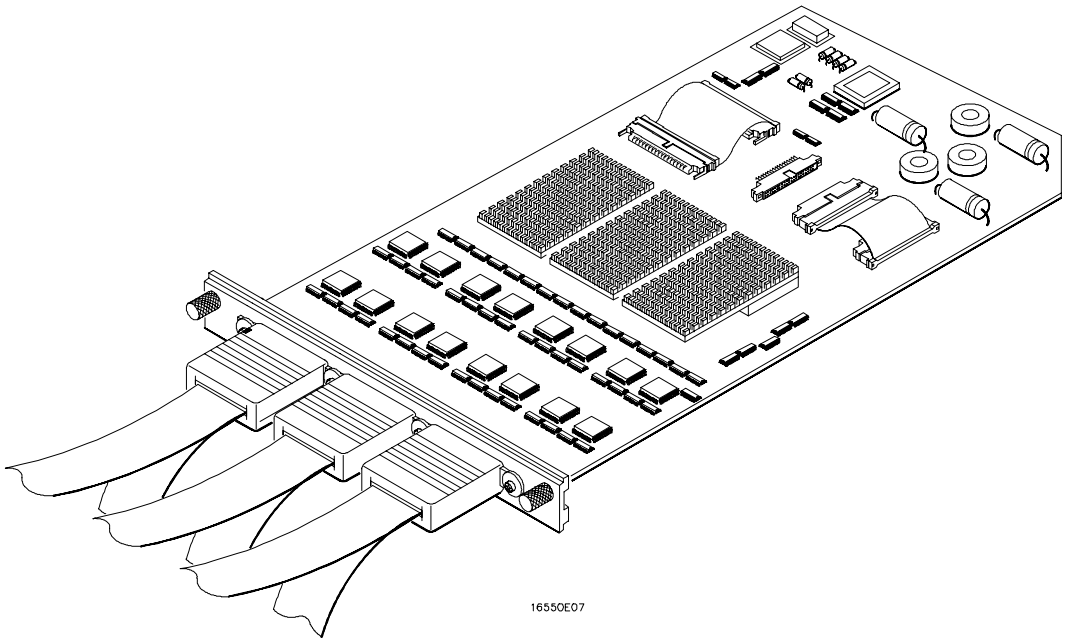
Some of the main features of the HP 16550A are as follows:

- 96 data channels
- 6 clock/data channels
- 4K memory depth per channel
- 100 MHz maximum state acquisition speed
- 500 MHz maximum timing acquisition speed
- Expandable to 204 channels

Service Strategy

The service strategy for this instrument is the replacement of defective assemblies. This service guide contains information for finding a defective assembly by testing and servicing the HP 16550A state and timing analyzer module.

This module can be returned to Hewlett-Packard for all service work, including troubleshooting. Contact your nearest Hewlett-Packard Sales Office for more details.



The HP 16550A 100-MHz State/500-MHz Timing Logic Analyzer

In This Book

This book is the service guide for the HP 16550A 100-MHz State/500-MHz Timing Logic Analyzer module. Place this service guide in the 3-ring binder supplied with your *HP 16500A Logic Analysis System Service Manual*.

This service guide is divided into eight chapters.

Chapter 1 contains information about the module and includes accessories for the module, specifications and characteristics of the module, and a list of the equipment required for servicing the module.

Chapter 2 tells how to prepare the module for use.

Chapter 3 gives instructions on how to test the performance of the module.

Chapter 4 contains calibration instructions for the module.

Chapter 5 contains self-tests and flowcharts for troubleshooting the module.

Chapter 6 tells how to replace the module and assemblies of the module and how to return them to Hewlett-Packard.

Chapter 7 lists replaceable parts, shows an exploded view, and gives ordering information.

Chapter 8 explains how the analyzer works and what the self-tests are checking.

Contents

6 Replacing Assemblies

7 Replaceable Parts

8 Theory of Operation

1

General Information

General Information

This chapter lists the accessories, the specifications and characteristics, and the recommended test equipment.

Accessories

The following accessories are supplied with the HP 16550A logic analyzer.

Accessories Supplied	HP Part Number
Probe Tip Assembly, Qty 6	01650-61608
Grabbers, Qty 6 packages	5090-4356
Extra Probe Leads, Qty 1 package	5959-9333
Probe Cable ID Clip, Qty 1	16500-41201
Probe Cables, Qty 3	16550-61601
Probe Cable and Pod Labels, Qty 1	01650-94310

Accessories Available

The accessories available for the HP 16550A are listed in the *Accessories for HP Logic Analyzers* brochure.

Specifications

The specifications are the performance standards against which the product is tested.

Maximum State Speed	100 MHz
Minimum State Clock Pulse Width*	3.5 ns
Minimum Master to Master Clock Time*	10.0 ns
Minimum Glitch Width	3.5 ns
Threshold Accuracy	± (100 mV + 3% of threshold setting)
Setup/Hold Time:*	
Single Clock, Single Edge	0.0/3.5 ns through 3.5/0.0 ns, adjustable in 500-ps increments
Single Clock, Multiple Edges	0.0/4.0 ns through 4.0/0.0 ns, adjustable in 500-ps increments
Multiple Clocks, Multiple Edges	0.0/4.5 ns through 4.5/0.0 ns, adjustable in 500-ps increments

* Specified for an input signal VH = –0.9 V, VL = –1.7 V, slew rate = 1 V/ns, and threshold = –1.3 V.

Characteristics

The characteristics are not specifications, but are included as additional information.

	Full Channel	**Half Channel**
Maximum State Clock Rate	100 MHz	100 MHz
Maximum Conventional Timing Rate	250 MHz	500 MHz
Maximum Transitional Timing Rate	125 MHz	250 MHz
Maximum Timing with Glitch Rate	N/A	125 MHz
Channel Count*	102/204	51/102
Memory Depth	4K	8K**

*Channel count is doubled when two HP 16550A cards are connected together.

**For all modes except glitch.

Supplemental Characteristics

Probes

Input Resistance	100 kΩ, ± 2%
Input Capatiance	~ 8 pF
Minimum Voltage Swing	500 mV, peak-to-peak
Threshold Range	± 6.0 V, adjustable in 50-mV increments

State Analysis

State/Clock Qualifiers	6
Time Tag Resolution*	8 ns
Maximum Time Count Between States	34 seconds
Maximum State Tag Count*	4.29×10^9

Timing Analysis

Sample Period Accuracy	0.01 % of sample period
Channel-to-Channel Skew	2 ns, typical
Time Interval Accuracy	± [sample period + channel-to-channel skew +(0.01%)(time reading)]

Triggering

Sequencer Speed	125 MHz, maximum
State Sequence Levels	12
Timing Sequence Levels	10
Maximum Occurrence Counter Value	1,048,575
Pattern Recognizers	10
Maximum Pattern Width	102 channels in a one-card configuration. 204 channels in a two-card configuration.
Range Recognizers	2
Range Width	32 bits each
Timers	2
Timer Value Range	400 ns to 500 seconds
Glitch/Edge Recognizers	2 (timing only)
Maximum Glitch/Edge Width	102 channels in a one-card configuration. 204 channels in a two-card configuration.

*Maximum state clock rate with time or state tags on is 100 MHz. When all pods are assigned to a state or timing machine, time or state tags halve the memory depth.

Measurement and Display Functions

Arming Each module can be armed by the RUN key, by the external PORT IN, or by another module via the Intermodule Bus (IMB).

Displayed Waveforms 24 lines maximum, with scrolling across 96 waveforms.

Measurement Functions

Run/Stop Functions Run Starts acquisition of data in specified trace mode.

Stop In single trace mode or the first run of a repetitive acquisition, STOP halts acquisition and displays the current acquisition data. For subsequent runs in repetitive mode, STOP halts acquisition of data and does not change the current display.

Trace Mode Single mode acquires data once per trace specification. Repetitive mode repeats single mode acquisitions until stop is pressed or until the time interval between two specified patterns is less than or greater than a specified value, or within or not within a specified range.

Indicators

Activity Indicators Provided in the Configuration and Format menus for identifying high, low, or changing states on the inputs.

Markers Two markers (X and 0) are shown as dashed lines on the display.

Trigger Displayed as a vertical dashed line in the Timing Waveform display and as line 0 in the State Listing display.

Data Entry/Display

Labels Channels may be grouped together and given a 6-character name. Up to 126 labels in each analyzer may be assigned with up to 32 channels per label.

Display Modes State listing, State Waveforms, Chart, Compare Listing, Compare Difference Listing, Timing Waveforms, and Timing Listings. State Listing, Timing Waveforms and Oscilloscope Waveforms can be time-correlated on the same displays.

Timing Waveform Pattern readout of timing waveforms at X or 0 marker.

Bases Binary, Octal, Decimal, Hexadecimal, ASCII (display only), Two's Complement, and User-defined symbols.

Symbols 1,000 maximum. Symbols can be downloaded over RS-232 or HP-IB.

Marker Functions

Time Interval The X and 0 markers measure the time interval between one point on a timing waveform and trigger, two points on the same timing waveform, two points on different waveforms, or two states (time tagging on).

Delta States (state analyzer only) The X and 0 markers measure the number of tagged states between one state and trigger or between two states.

Patterns The X and 0 markers can be used to locate the *nth* occurrence of a specified pattern from trigger, or from the beginning of data. The 0 marker can also find the *nth* occurrence of a pattern from the X marker.

Statistics X and 0 marker statistics are calculated for repetitive acquisitions. Patterns must be specified for both markers and statistics are kept only when both patterns can be found in an acquisition. Statistics are minimum X to 0 time, maximum X to 0 time, average X to 0 time, and ratio of valid runs to total runs.

Auxiliary Power

Power Through Cables	1/3 amp at 5 V maximum per cable

Operating Environment

Temperature	Instrument, 0 °C to 55 °C (+32 °F to 131 °F). Probe lead sets and cables, 0 °C to 65 °C (+32 °F to 149 °F).
Humidity	Instrument, probe lead sets, and cables, up to 95% relative humidity at +40 °C (+122 °F).
Altitude	To 4600 m (15,000 ft).
Vibration	**Operating: Random vibration 5 to 500 Hz, 10 minutes per axis,** ≈0.3 g (rms). Non-operating: Random vibration 5 to 500 Hz, 10 minutes per axis, ≈ 2.41 g (rms); and swept sine resonant search, 5 to 500 Hz, 0.75 g (0-peak), 5 minute resonant dwell at 4 resonances per axis.

Recommended Test Equipment

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part	Use*
Pulse Generator	100 MHz, 3.5 ns pulse width, < 600 ps rise time	HP 8131A Option 020	P,T
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	HP 54121T	P
Function Generator	Accuracy $\leq(5)(10^{-6}) \times$ frequency, DC offset voltage ±6.3 V	HP 3325B Option 002	P
Digital Multimeter	0.1 mV resolution, 0.005% accuracy	HP 3458A	P
BNC-Banana Cable		HP 11001-60001	P
BNC Tee	BNC (m)(f)(f)	HP 1250-0781	P
Cable	BNC (m-m) 48 inch	HP 10503A	P
SMA Coax Cable (Qty 3)	≥ 18 GHz bandwidth	HP 8120-4948	P
Adapter (Qty 4)	SMA(m)-BNC(f)	HP 1250-1200	P
Adapter	SMA(f)-BNC(m)	HP 1250-2015	P
Coupler	BNC (m-m)	HP 1250-0216	P
20:1 Probes (Qty 2)		HP 54600A	P
BNC Test Connector, 17x2 (Qty 1)**			P
BNC Test Connector, 6x2 (Qty 4)**			P,T

*A = Adjustment P = Performance Tests T = Troubleshooting

**Instructions for making these test connectors are in chapter 3, "Testing Performance."

2

Preparing for Use

Preparing For Use

This chapter gives you instructions for preparing the logic analyzer module for use.

Power Requirements

All power supplies required for operating the logic analyzer are supplied through the backplane connector in the mainframe.

Operating Environment

The operating environment is listed in chapter 1. Note the non-condensing humidity limitation. Condensation within the instrument can cause poor operation or malfunction. Provide protection against internal condensation.

The logic analyzer module will operate at all specifications within the temperature and humidity range given in chapter 1. However, reliability is enhanced when operating the module within the following ranges:

- Temperature: +20 °C to +35 °C (+68 °F to +95 °F)
- Humidity: 20% to 80% non-condensing

Storage

Store or ship the logic analyzer in environments within the following limits:

- Temperature: -40 °C to + 75 °C
- Humidity: Up to 90% at 65 °C
- Altitude: Up to 15,300 meters (50,000 feet)

Protect the module from temperature extremes which cause condensation on the instrument.

To inspect the module

1. Inspect the shipping container for damage.

   If the shipping container or cushioning material is damaged, keep them until you have checked the contents of the shipment and checked the instrument mechanically and electrically.
2. Check the supplied accessories.

   Accessories supplied with the module are listed in chapter 1, "Accessories Supplied."
3. Inspect the product for physical damage.

   Check the module and the supplied accessories for obvious physical or mechanical defects. If you find any defects, contact your nearest Hewlett-Packard Sales Office. Arrangements for repair or replacement are made, at Hewlett-Packard's option, without waiting for a claim settlement.

To prepare the mainframe

CAUTION Turn off the mainframe power before removing, replacing, or installing the module.

CAUTION Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when performing any service to this module.

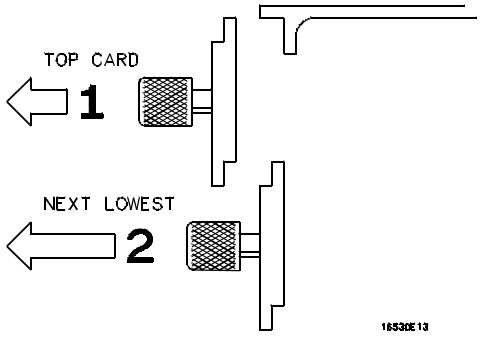
1. Turn off the mainframe power switch, then unplug the power cord. Disconnect any input or output connections.
2. Plan your module configuration.

   If you are installing a one-card module, use any available slot in the mainframe.

   If you are installing a two-card module, use two adjacent slots in the mainframe. The bottom card will be the master card of the module. Up to two, two-card modules can be installed in a mainframe.
3. Loosen the thumb screws.

   Cards or filler panels below the slots intended for installation do not have to be removed.

   Starting from the top, loosen the thumb screws on filler panels and cards that need to be moved.



4. Starting from the top, pull the cards and filler panels that need to be moved halfway out.

CAUTION All multicard modules will be cabled together. Pull these cards out together.

5. Remove the cards and filler panels.

   Remove the cards or filler panels that are in the slots intended for the module installation. Push all other cards into the card cage, but not completely in. This is to get them out of the way for installing the module.

CAUTION Some modules for the Logic Analysis System require calibration if you move them to a different slot. For calibration information, refer to the manuals for the individual modules.

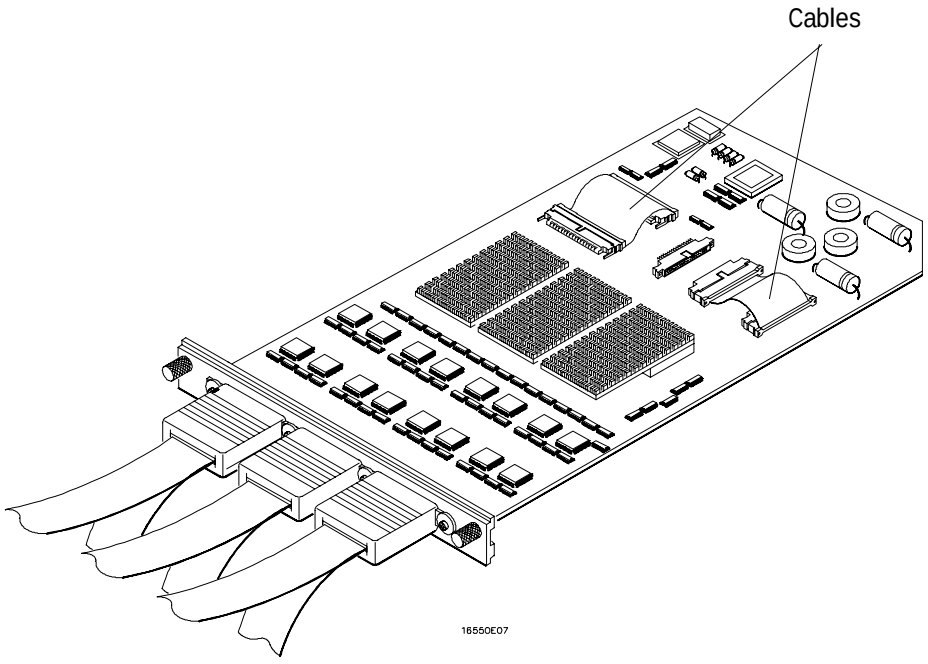
To configure a one-card module

- When shipped separately, the module is configured as a one-card module. The cables should be connected as shown in the figure.
- To configure a two-card module into a one-card module, remove the cables connecting the two cards, then co nnect the cables as shown.

CAUTION

If you pull on the flexible ribbon part of the cable, you might damage the cable assembly. To remove a cable from the cable connector on the board, gently pry the hard plastic part of the cable assembly away from the connector using a screwdriver.

Directions for connecting the cables are printed on the circuit board.



To configure a two-card module

Directions for connecting the cables are printed on the circuit board.

To configure a two-card module, connect the cables as follows.

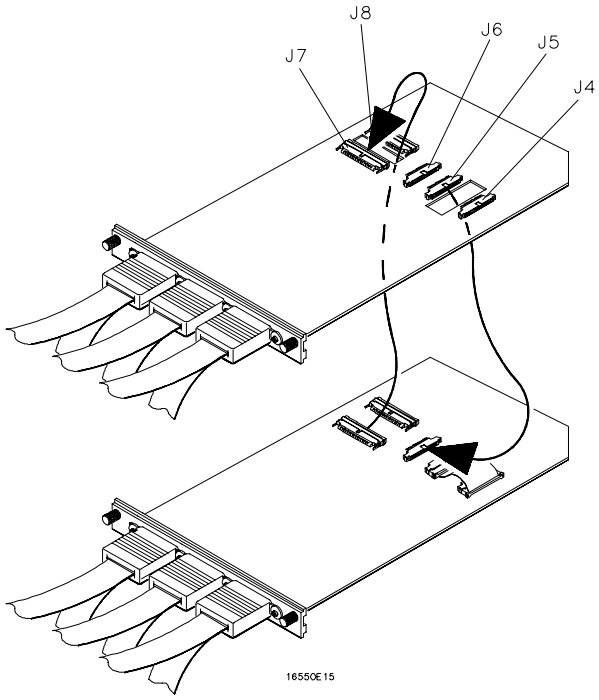
1. Disconnect the two cables from J4 and J5 and from J7 and J8 on the card to go in the upper slot.

CAUTION

If you pull on the flexible ribbon part of the cable, you might damage the cable assembly. To remove a cable from the cable connector on the board, gently pry the hard plastic part of the cable assembly away from the connector using a screwdriver.

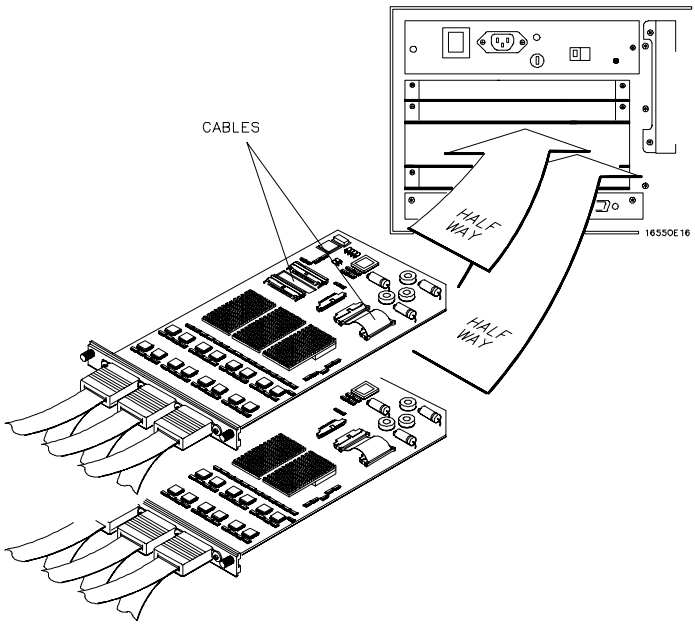
2. Disconnect the cable from J7 and J8 of the card to go in the lower slot.
3. Connect the 80-pin cable from J6 of the lower card to J5 of the upper card. The cable between J4 and J5 of the lower card should remain connected.
4. Connect the 100-pin cable from J7 of the lower card to J7 of the upper card.

Save unused cables for future configurations.



To install the module

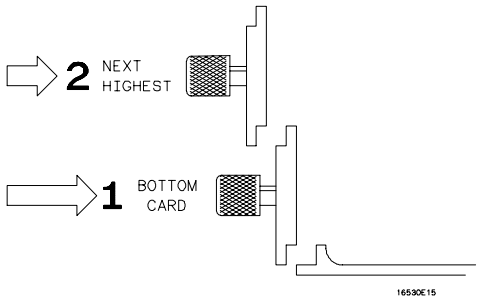
1. Slide the cards above the slots for the module about halfway out of the mainframe.
2. With the probe cables facing away from the instrument, slide the module approximately halfway into the mainframe.



3. Slide the complete module into the mainframe, but not completely in.

   Each card in the instrument is firmly seated and tightened one at a time in step 5.
4. Position all cards and filler panels so that the endplates overlap.
5. Seat the cards and tighten the thumbscrews.

   Starting with the bottom card, firmly seat the cards into the backplane connector of the mainframe. Keep applying pressure to the center of the card endplate while tightening the thumbscrews finger-tight. Repeat this for all cards and filler panels starting at the bottom and moving to the top.

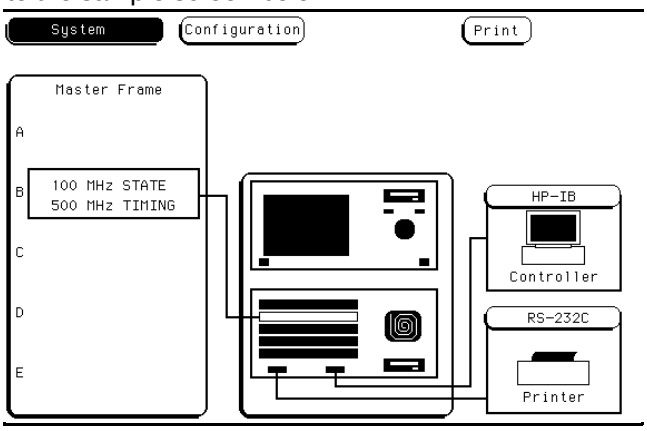


CAUTION Correct air circulation keeps the instrument from overheating. For correct air circulation, filler panels must be installed in all unused card slots. Keep any extra filler panels for future use.

To turn on the system

1. Connect the power cable to the mainframe.
2. Insert the disk containing the operating system a disk drive.
3. Turn on the instrument power switch.

   When you turn on the instrument power switch, the instrument performs powerup tests that check mainframe circuitry. After the powerup tests are complete, the screen will look similar to the sample screen below.



To test the module

The logic analyzer module does not require calibration or adjustment. After installing the module, you can test and use the module.

- If you require a test to verify the specifications, start at the beginning of chapter 3, "Testing Performance."
- If you require a test to initially accept the operation, perform the self-tests in chapter 3.
- If the module does not operate correctly, go to the beginning of chapter 5, "Troubleshooting."

3

Testing Performance

Testing Performance

This chapter tells you how to test the performance of the logic analyzer against the specifications listed in chapter 1. To ensure the logic analyzer is operating as specified, software tests (self-tests) and manual performance tests are done on the module. The logic analyzer is considered performance-verified if all of the software tests and manual performance tests have passed. The procedures in this chapter indicate what constitutes a "Pass" status for each of the tests.

Test Strategy

For a complete test, start at the beginning with the software tests and continue through to the end of the chapter. For an individual test, follow the procedure in the test.

One-card module

To perform a complete test on a one-card module, start at the beginning of the chapter and follow each procedure.

Two-card module

To perform a complete test on a two-card module, perform the software tests with the cards connected. Then, remove the two-card module from the mainframe and configure each card as a one-card module. Install the one-card modules into the mainframe and perform the one-card manual performance tests on each card. When the tests are complete, remove the one-card modules, reconfigure them into two-card modules, reinstall them into the mainframe, then perform the final two-card test. For removal instructions, see chapter 6, "Replacing Assemblies." For installation and configuration instructions, see chapter 2, "Preparing for Use."

Test Interval

Test the performance of the module at two-year intervals or if it is replaced or repaired.

Test Record Description

A performance test record for recording the results of each procedure is located at the end of this chapter. Use the performance test record to gauge the performance of the module over time.

Test Equipment

Each procedure lists the recommended test equipment. You can use equipment that satisfies the specifications given. However, the procedures are based on using the recommended model or part number.

Instrument Warm-Up

Before testing the performance of the module, warm-up the instrument and the test equipment for 30 minutes.

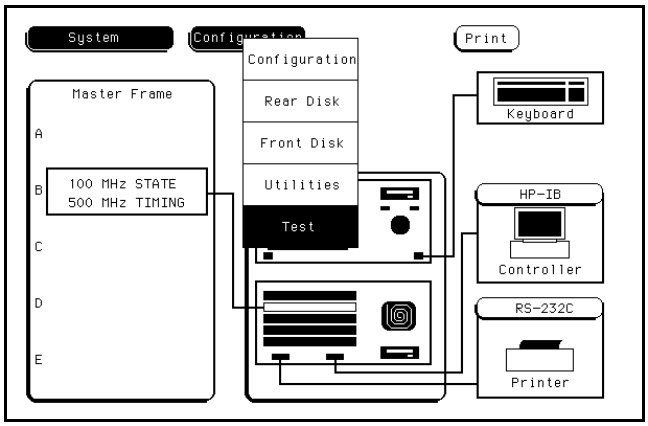
To perform the self-tests and make the test connectors

The self-tests verify the correct operation of the logic analyzer module. Self-tests can be performed all at once or one at a time. While testing the performance of the module, run the self-test all at once.

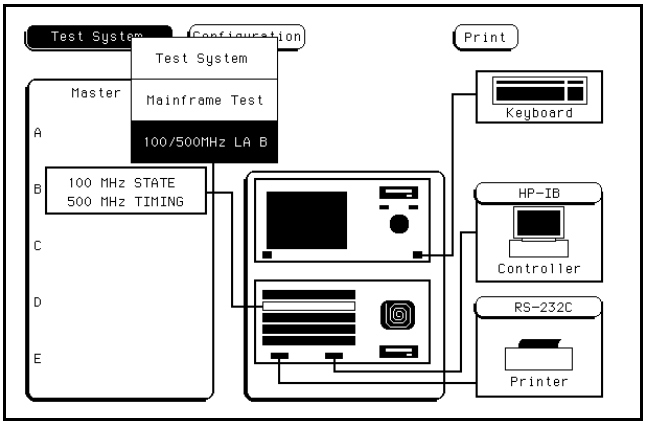
The test connectors connect the analyzer to the test equipment.

Perform the self-tests

1. Disconnect all inputs, insert the disk containing the operating system into a disk drive, then turn on the power switch.
2. In the System Configuration menu, touch Configuration. In the pop-up, touch Test.

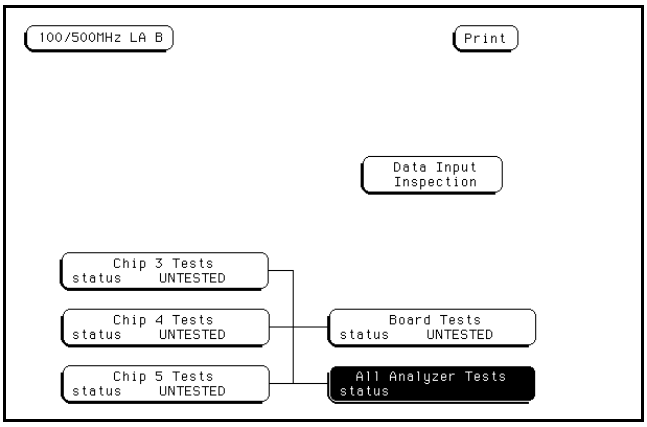


3. Remove the disk containing the operating system, then insert the disk containing the performance verification (self-tests) into the disk drive. Touch the box labeled Touch box to Load Test System.
4. On the test system screen, touch Test System. Select the 100 MHz/500 MHz LA module to be tested.



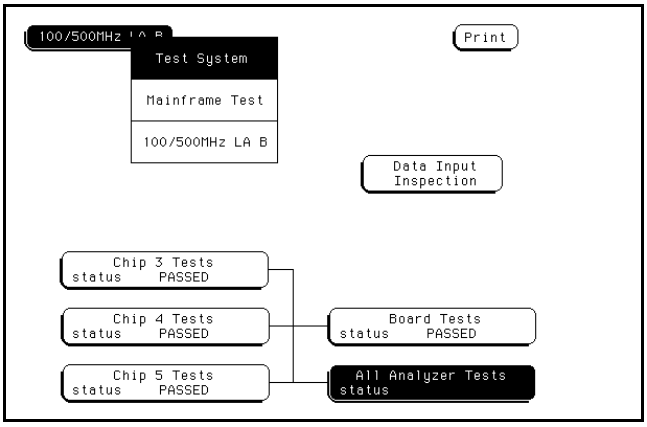
5 Touch All Analyzer Tests.

You can run all tests at one time by touching All Analyzer Tests. To see more details about each test when troubleshooting failures, you can run each test individually. This example shows how to run all tests at once.



6 When the tests finish, the status will show Passed or Failed. Record the results of the test on the performance test record at the end of this chapter.

7 Touch 100/500 MHz LA. If more logic analyzer cards are to be tested, select the next card, then repeat the test. When all cards are tested, touch 100/500 MHz, then select Test System.



8 Touch Configuration, then select Exit Test. Remove the disk containing the performance verification test, then insert the disk containing the operating system. Touch the box labeled Touch box to Exit Test System.

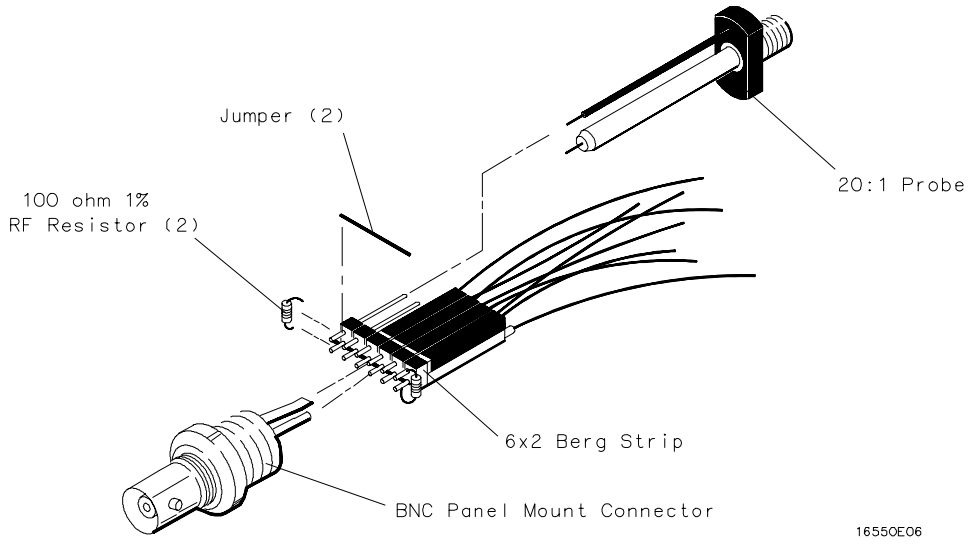
Make the test connectors

Materials Required

Description	Recommended Part	Qty
BNC (f) Connector	HP 1250-1032	5
100 Ω 1% resistor	HP 0698-7212	8
Berg Strip, 17-by-2		1
Berg Strip, 6-by-2		4
20:1 Probe	HP 54006A	2
Jumper wire		

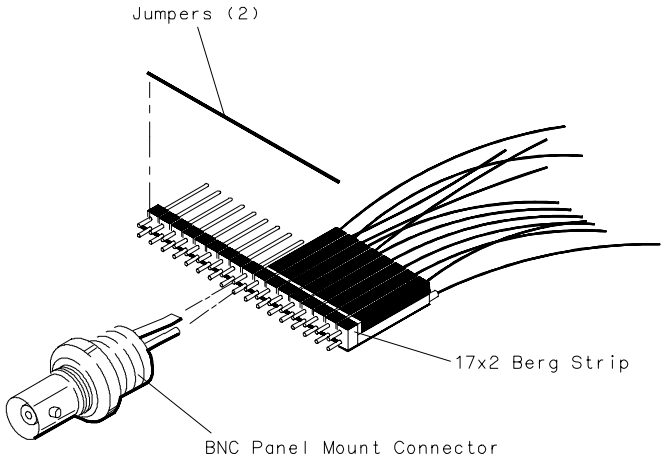
1 Build four test connectors using BNC connectors and 6-by-2 sections of Berg strip.

- **a** Solder a jumper wire to all pins on one side of the Berg strip.
- **b** Solder a jumper wire to all pins on the other side of the Berg strip.
- **c** Solder two resistors to the Berg strip, one at each end between the end pins.
- **d** Solder the center of the BNC connector to the center pin of one row on the Berg strip.
- **e** Solder the ground tab of the BNC connector to the center pin of the other row on the Berg strip.
- **f** On two of the test connectors, solder a 20:1 probe. The probe ground goes to the same row of pins on the test connector as the BNC ground tab.



2 Build one test connector using a BNC connector and a 17-by-2 section of Berg strip.

- **a** Solder a jumper wire to all pins on one side of the Berg strip.
- **b** Solder a jumper wire to all pins on the other side of the Berg strip.
- **c** Solder the center of the BNC connector to the center pin of one row on the Berg strip.
- **d** Solder the ground tab of the BNC connector to the center pin of the other row on the Berg strip.



1655OEO5

To test the threshold accuracy

Testing the threshold accuracy verifies the performance of the following specification:

- Clock and data channel threshold accuracy.

Two-card modules must be reconfigured as one-card modules for this test.

These instructions include detailed steps for testing the threshold settings of pod 1. After testing pod 1, connect and test the rest of the pods one at a time. To test the next pod, follow the detailed steps for pod 1, substituting the next pod for pod 1 in the instructions.

Equipment Required

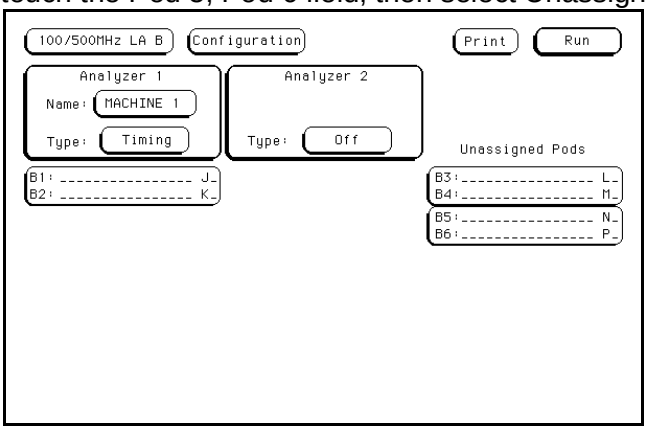
Equipment	Critical Specifications	Recommended Model/Part
Digital Multimeter	0.1 mV resolution, 0.005% accuracy	HP 3458A
Function Generator	Accuracy $\leq (5)(10^{-6}) \times$ frequency, DC offset voltage ± 6.3 V	HP 3325B Option 002
BNC-Banana Cable		HP 11001-60001
BNC Tee		HP 1250-0781
BNC Cable		HP 10503A
BNC Test Connector, 17x2		

Set up the equipment

1. Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes before beginning the test.
2. Set up the function generator.
   - **a** Set up the function generator to provide a DC offset voltage at the Main Signal output.
   - **b** Disable any AC voltage to the function generator output, and enable the high voltage output.
   - **c** Monitor the function generator DC output voltage with the multimeter.

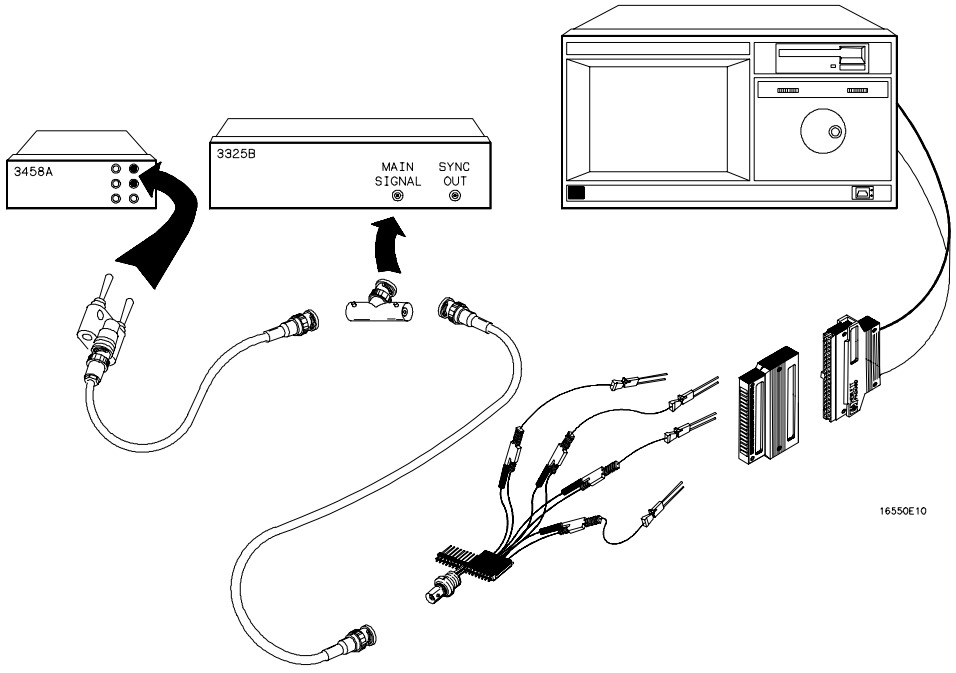
Set up the logic analyzer

1. In the System Configuration menu, touch System, then select 100/500 MHz LA.
2. In the Configuration menu, unassign Pod 5 and Pod 6. To unassign the pods, touch the Pod 5, Pod 6 field, then select Unassigned.



Connect the logic analyzer

1. Using the 17-by-2 test connector, BNC cable, and probe tip assembly, connect the data and clock channels of pod 1 to one side of the BNC Tee.
2. Using a BNC-banana cable, connect the voltmeter to the other side of the BNC Tee.
3. Connect the BNC Tee to the Main Signal output of the function generator.

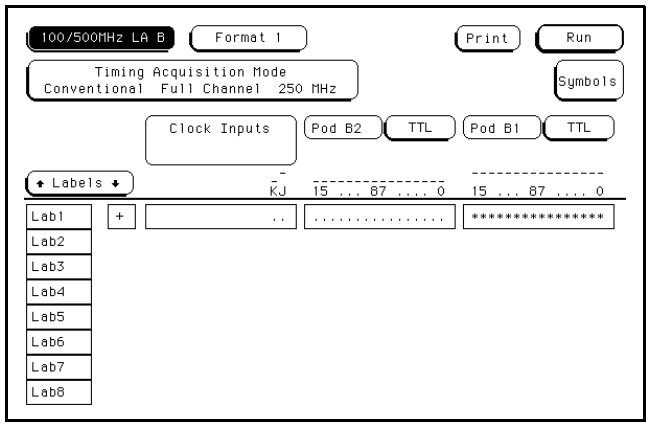


Test the TTL threshold

1 In the Configuration menu, touch Configuration, then touch Format. In the Format menu, touch the field to the right of Pod 1, then select TTL.

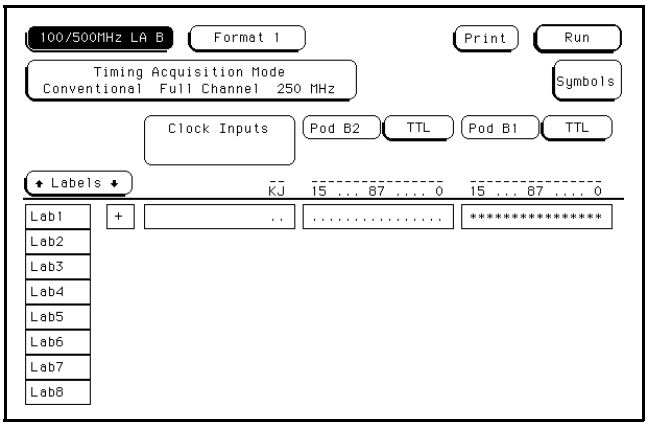
2 On the function generator front panel, enter 1.750 V ±1 mV DC offset. Use the multimeter to verify the voltage.

The activity indicators for pod 1 should show all data channels and the J-clock channel at a



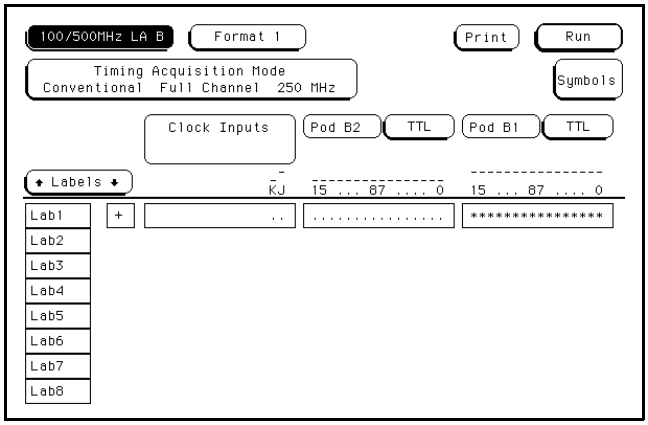
logic high.

3 Using the Modify down arrow on the function generator, decrease offset voltage in



1-mV increments until all activity indicators for pod 1 show the channels at a logic low. Record the function generator voltage in the performance test record.

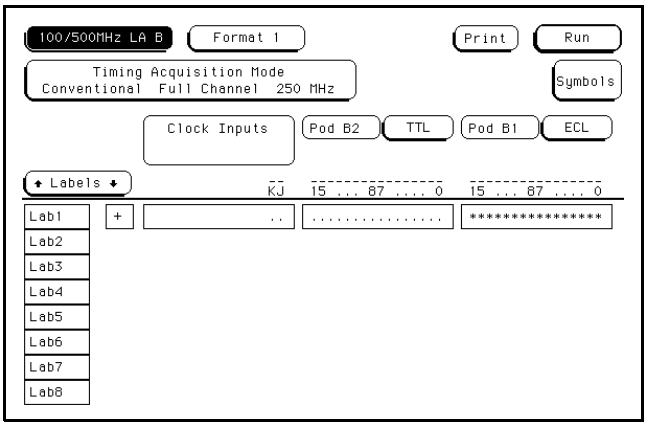
4 Using the Modify up arrow on the function generator, increase offset voltage in 1-mV increments until all activity indicators for pod 1 show the channels at a logic high. Record the function generator voltage in the performance test record.



Test the ECL threshold

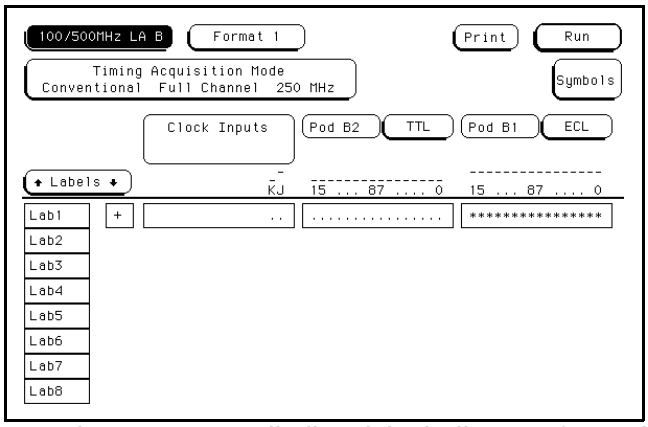
1. In the Format menu, touch the field to the right of Pod 1, then select ECL.
2. On the function generator front panel, enter –1.160 V ±1 mV DC offset. Use the multimeter to verify the voltage.

   The activity indicators for pod 1 should show all data channels and the J-clock channel at a logic high.
3. Using the Modify down arrow on the function generator, decrease offset voltage in 1-mV increments until all activity indicators for pod 1 show the channels are at a



logic low. Record the function generator voltage in the performance test record.

4. Using the Modify up arrow on the function generator, increase offset voltage in

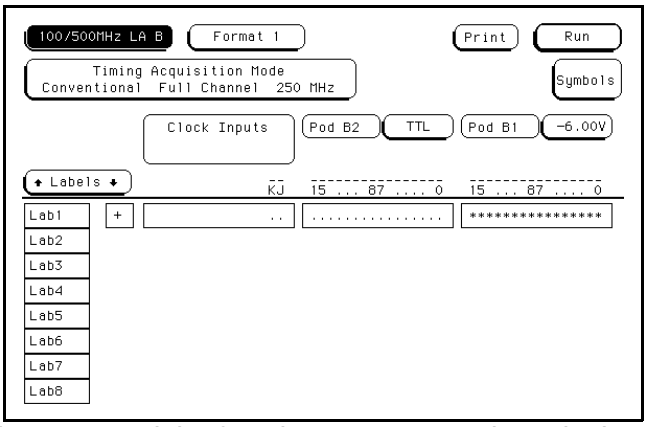


1-mV increments until all activity indicators for pod 1 show the channels are at a logic high. Record the function generator voltage in the performance test record.

Test the – User threshold

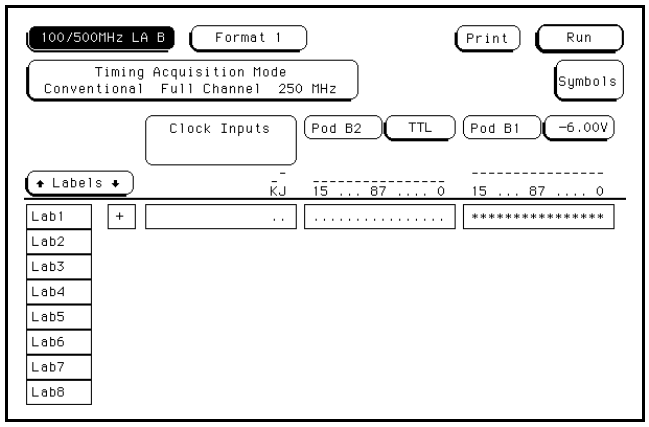
1. In the Format menu, touch the field to the right of Pod 1, then select User. In the pop-up menu, enter –6.00 V, then touch Done.
2. On the function generator front panel, enter –5.718 V ±1 mV DC offset. Use the multimeter to verify the voltage.

   The activity indicators for pod 1 should show all data channels and the J-clock channel at a logic high.
3. Using the Modify down arrow on the function generator, decrease offset voltage in 1-mV increments until all activity indicators for pod 1 show the channels at a logic



low. Record the function generator voltage in the performance test record.

4. Using the Modify up arrow on the function generator, increase offset voltage in

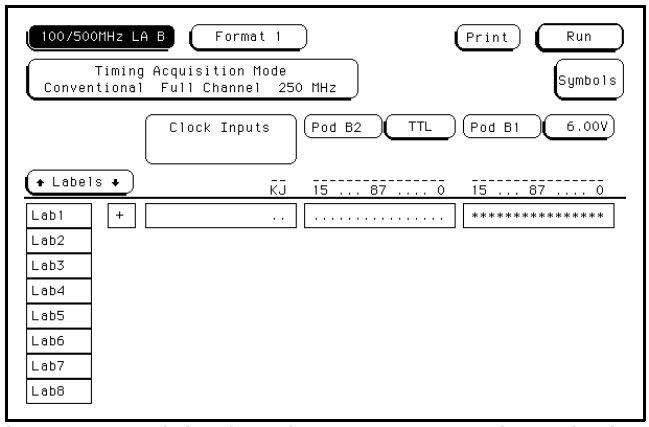


1-mV increments until all activity indicators show the channels at a logic high. Record the function generator voltage in the performance test record.

Test the + User threshold

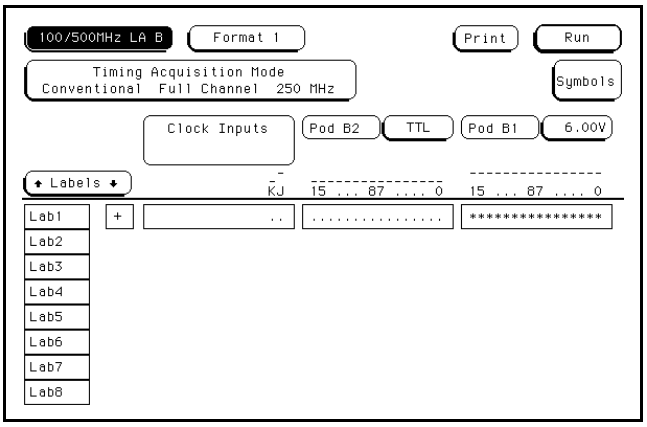
1. In the Format menu, touch the field to the right of Pod 1, then select User. In the pop-up menu, enter +6.00 V, then touch Done.
2. On the function generator front panel, enter +6.282 V ±1 mV DC offset. Use the multimeter to verify the voltage.

   The activity indicators for pod 1 should show all data channels and the J-clock channel at a logic high.
3. Using the Modify down arrow on the function generator, decrease offset voltage in 1-mV increments until all activity indicators for pod 1 show the channels at a logic



low. Record the function generator voltage in the performance test record.

4. Using the Modify up arrow on the function generator, increase offset voltage in

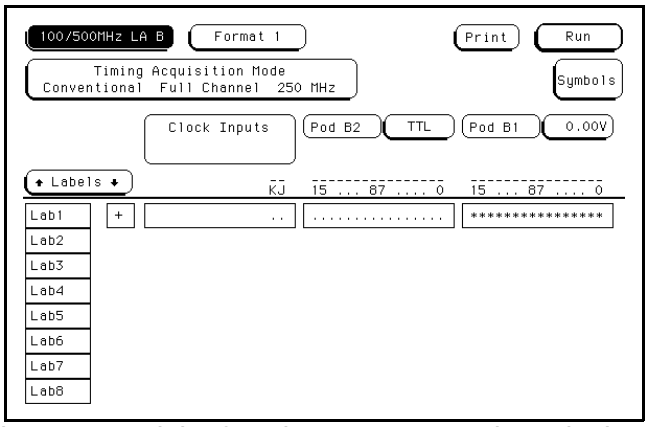


1-mV increments until all activity indicators for pod 1 show the channels at a logic high. Record the function generator voltage in the performance test record.

Test the 0 V User threshold

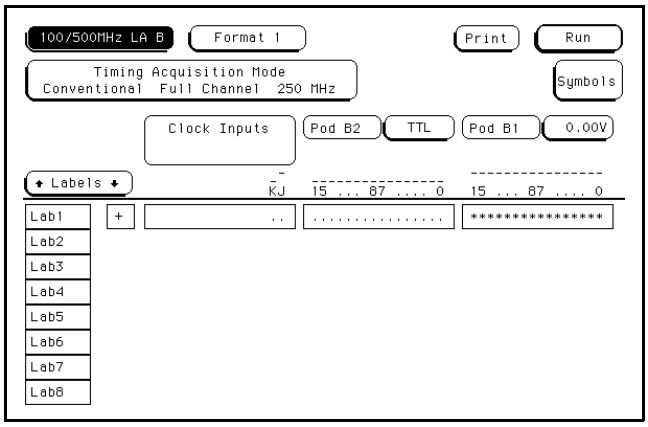
1. In the Format menu, touch the field to the right of Pod 1, then select User. In the pop-up menu, enter 0.00 V, then touch Done.
2. On the function generator front panel, enter +0.102 V ±1 mV DC offset. Use the multimeter to verify the voltage.

   The activity indicators for pod 1 should show all data channels and the J-clock channel at a logic high.
3. Using the Modify down arrow on the function generator, decrease offset voltage in 1-mV increments until all activity indicators for pod 1 show the channels at a logic



low. Record the function generator voltage in the performance test record.

4. Using the Modify up arrow on the function generator, increase offset voltage in



1-mV increments until all activity indicators for pod 1 show the channels at a logic high. Record the function generator voltage in the performance test record.

Test the next pod

Using the 17-by-2 test connector and probe tip assembly, connect the data and clock channels of the next pod to the output of the function generator.

- If you just finished testing pod 1, connect the data and clock channels of pod 2. Start with "Test the TTL threshold" on page 3–9, substituting pod 2 for pod 1.
- If you just finished testing pod 2, connect the data and clock channels of pod 3. In the logic analyzer Configuration menu, unassign pods 1 and 2, assign pods 3 and 4 to Machine 1. Start with "Test the TTL threshold" on page 3–9, substituting pod 3 for pod 1.
- If you just finished testing pod 3, connect the data and clock channels of pod 4. Start with "Test the TTL threshold" on page 3–9, substituting pod 4 for pod 1.
- If you just finished testing pod 4, connect the data and clock channels of pod 5. In the logic analyzer Configuration menu, unassign pods 3 and 4, then assign pods 5 and 6 to Machine 1. Start with "Test the TTL threshold" on page 3–9, substituting pod 5 for pod 1.
- If you just finished testing pod 5, connect the data and clock channels of pod 6. Start with "Test the TTL threshold" on page 3–9, substituting pod 6 for pod 1.
- If you just finished testing pod 6, you have completed the threshold accuracy test.

To test the glitch capture

Testing the glitch capture verifies the performance of the following specification:

- Minimum detectable glitch.

Two-card modules must be reconfigured as one-card modules for this test.

This test checks the minimum detectable glitch on sixteen data channels at a time.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	100 MHz 3.5 ns pulse width, < 600 ps rise time	HP 8131A Option 020
Digitizing Oscilloscope	≥ 6 GHz bandwidth , <58 ps rise time	HP 54121T
SMA Coax (Qty 3)		HP 8120-4948
Adapter (Qty 4)	SMA(m)-BNC(f)	HP 1250-1200
Coupler (Qty 4)	BNC m-m	HP 1250-0216
BNC Test Connector, 6x2 (Qty 4)		

Set up the equipment

1. Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes before beginning the test if you have not already done so.
2. Set up the pulse generator.

Pulse Generator Setup

Channel 1	Channel 2	Period
Delay: 0 ps	Delay : 0 ps	22.0 ns
Width: 3.5 ns	Width: 3.5 ns	
High: –0.9 V	High: –0.9 V	
Low: –1.7 V	Low: –1.7 V	

3 Set up the oscilloscope.

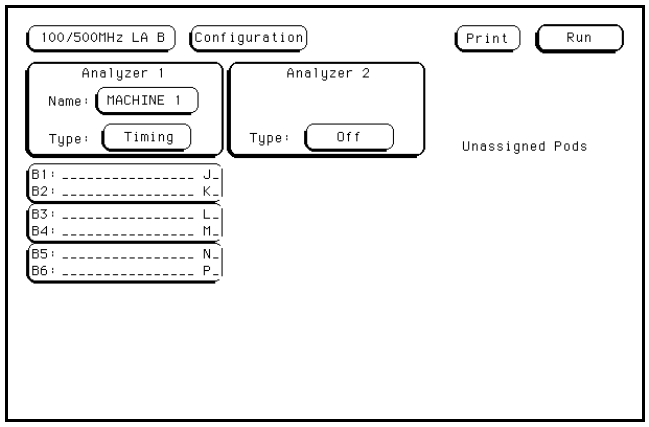
Oscilloscope Setup

Time Base	**Display**	**Delta V**	**Delta t**
Time/Div: 1.00 ns/div	mode: avg	V markers on	T markers on
delay: 17.7000 ns	# of avg: 16	marker 1 position: Chan 1	start on: Pos Edge 1
	screens: dual	marker 2 position: Chan 2	stop on: Pos Edge 1

	Channel 1	**Channel 2**
Display	on	on
Probe Atten	20.00	20.00
Volts/Div	400 mV	400 mV
Offset	–1.3000 V	–1.3000 V

Set up the logic analyzer

1 In the System Configuration menu, touch System, then select 100/500 MHz LA.
2 Touch the pod fields, then select Machine 1.
3 In the Analyzer 1 box, touch the Type field, then select Timing.

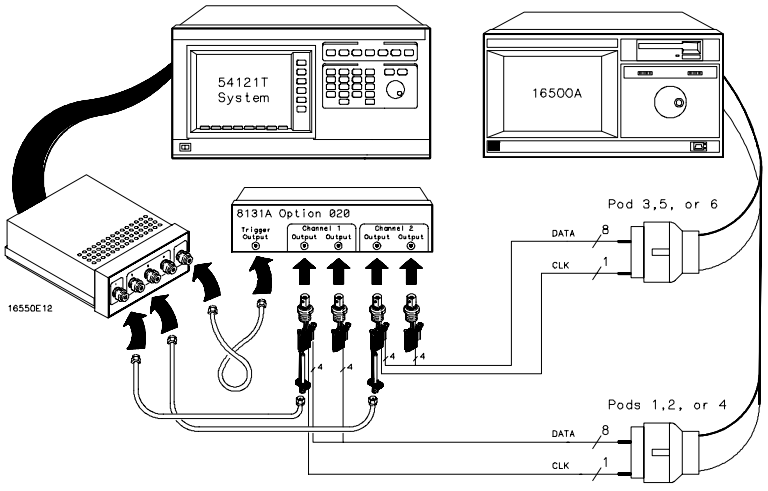


Connect the logic analyzer

1. Using 6-by-2 test connectors, connect the first combination of logic analyzer clock and data channels listed in the table below to the pulse generator.
2. Using SMA cables, connect channel 1, channel 2, and trigger from the oscilloscope to the pulse generator.

Connect the Logic Analyzer to the Pulse Generator

Testing Combinations	Connect to HP 8131A Channel 1 Output	Connect to HP 8131A _____ Channel 1 Output	Connect to HP 8131A Channel 2 Output	Connect to HP 8131A _____ Channel 2 Output
1	Pod 1, ch 0, 2, 4, 6, J-clock	Pod 1, ch 1, 3, 5, 7	Pod 3, ch 0, 2, 4, 6, L-clock	Pod 3, ch 1, 3, 5, 7
2	Pod 1, ch 8, 10, 12, 14, J-clock	Pod 1, ch 9, 11, 13, 15	Pod 3, ch 8, 10, 12, 14, L-clock	Pod 3, ch 9, 11, 13, 15
3	Pod 4, ch 0, 2, 4, 6, M-clock	Pod 4, ch 1, 3, 5, 7	Pod 6, ch 0, 2, 4, 6, P-clock	Pod 6, ch 1, 3, 5, 7
4	Pod 4, ch 8, 10, 12, 14, M-clock	Pod 4, ch 9, 11, 13, 15	Pod 6, ch 8, 10, 12, 14, P-clock	Pod 6 ch 9, 11, 13, 15
5	Pod 2, ch 0, 2, 4, 6, K-clock	Pod 2, ch 1, 3, 5, 7	Pod 5, ch 0, 2, 4, 6, N-clock	Pod 5, ch 1, 3, 5, 7
6	Pod 2, ch 8, 10, 12, 14, K-clock	Pod 2, ch 9, 11, 13, 15	Pod 5, ch 8, 10, 12, 14, N-clock	Pod 5, ch 9, 11, 13, 15



Test the glitch capture on the connected channels

1 Set up the Format menu.

a In the Configuration menu, touch Configuration, then touch Format.

b Touch the field to the right of each pod, then select ECL. Use the knob to access the pods not shown on screen.

c Touch Timing Acquisition Mode, then select Glitch Half Channel 125 MHz.

d Touch Lab1, then select Modify Label. In the pop-up, type Glitch, then touch Done. Touch Lab2, then select Modify Label. In the pop-up, type CLK, then touch Done.

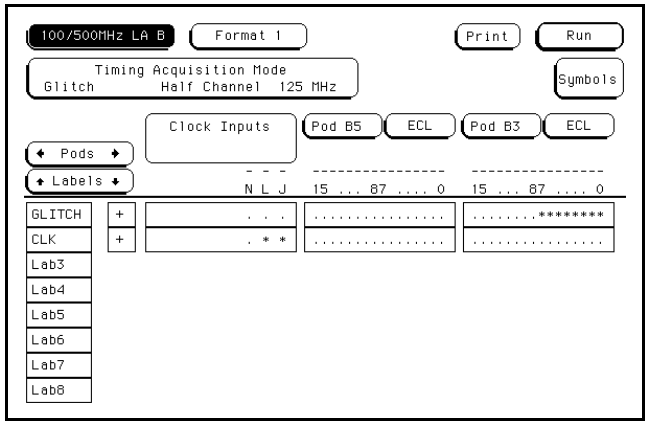
2 Turn on the channels that correspond to the channels being tested.

The channels being tested are the channels connected to the pulse generator in "Connect the logic analyzer."

a To access a pod, touch a pod field, then select one of the two pods in the pop-up.

b To turn on the channels of the selected pod, touch the channel field for the pod, then touch Clear in the pop-up. Use the knob to select the channel then touch the asterisk. Touch Done. Access and turn on the channels of the next pod being tested.

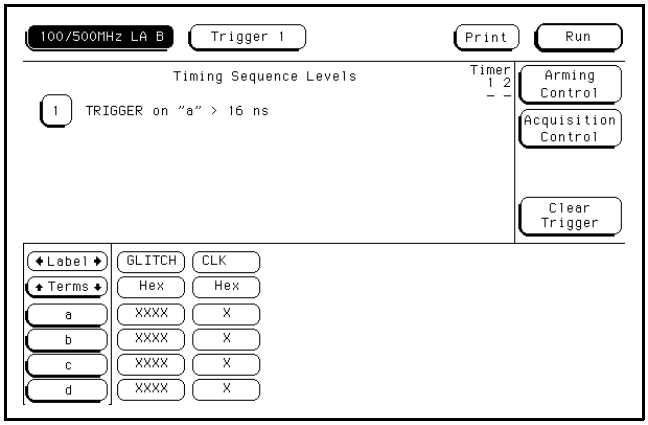
c Turn on the clock/data channels that correspond to the clocks being tested. Turn off the data channels and clock/data channels that are not being tested.



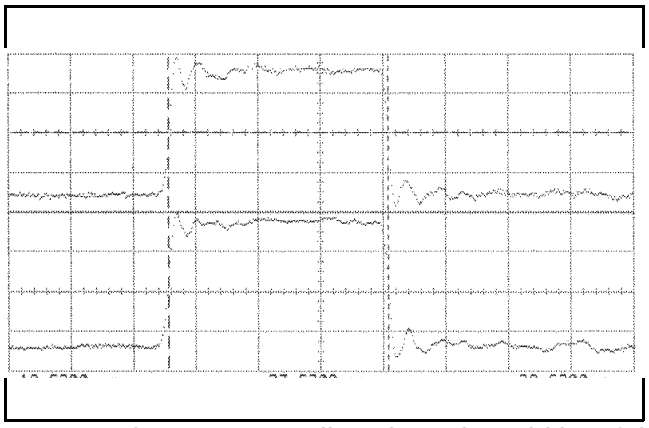
3 Set up the Trigger menu.

a Touch Format, then select Trigger.

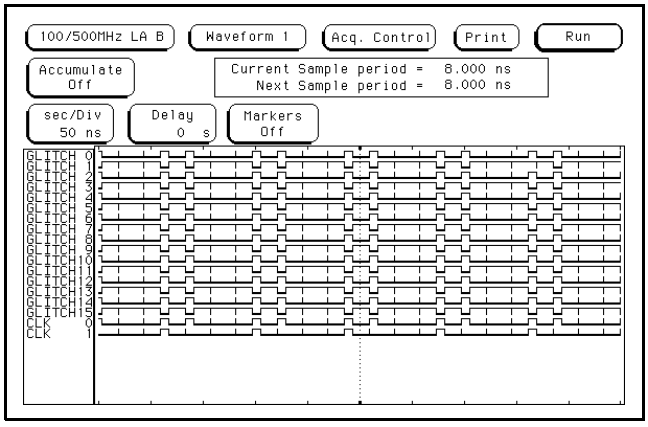
b In the Trigger menu, touch Clear Trigger, then select All.



4 Using the Precision Edge Find in the Delta t menu of the oscilloscope, verify that the pulse widths of the pulse generator channels 1 and 2 are 3.450 ns, +50 ps or



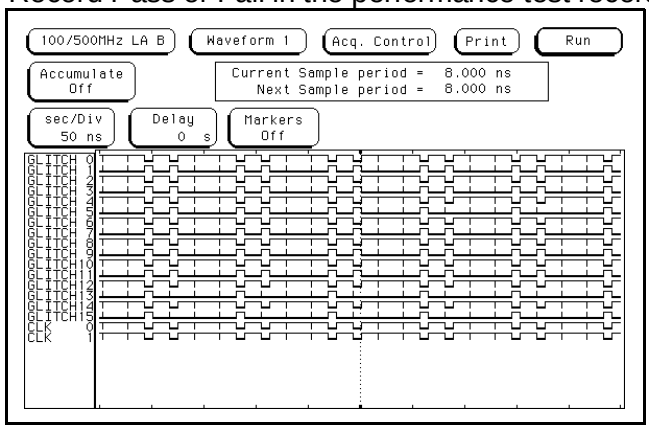
-100 ps. If necessary, adjust the pulse widths of the pulse generator channels 1 and 2.



5 On the logic analyzer, touch Run. The display should be similar to the figure below.

6 On the pulse generator, enable Channel 1 and Channel 2 COMP (with the LED on).

7 On the logic analyzer, touch Run. The display should be similar to the figure below. Record Pass or Fail in the performance test record.



Test the next channels

- Return to "Connect the logic analyzer" on page 3–18 and connect and test the next combination of data and clock channels until all combinations are tested.

  To access pods 2, 4, and 6 in the Format menu, touch the pods 1, 3, and 5 fields in the Format menu to toggle the pods.

To test the single-clock, single-edge, state acquisition

Testing the single-clock, single-edge, state acquisition verifies the performance of the following specifications:

- Minimum master to master clock time.
- Maximum state acquisition speed.
- Setup/Hold time.
- Minimum clock pulse width.

Two-card modules must be reconfigured as one-card modules for this test.

This test checks two combinations of data channels using a single-edge clock at three selected setup/hold times.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	100 MHz 3.5 ns pulse width, <600 ps rise time	HP 8131A option 020
Digitizing Oscilloscope	≥ 6 GHz bandwidth, <58 ps rise time	HP 54121T
Adapter	SMA(m)-BNC(f)	HP 1250-1200
SMA Coax Cable (Qty 3)		HP 8120-4948
Coupler	BNC(m-m)	HP 1250-0216
BNC Test Connector, 6x2 (Qty 4)		

Set up the equipment

1 Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes before beginning the test if you have not already done so.

2 Set up the pulse generator.

a Set up the pulse generator according to the following table.

Pulse Generator Setup

Channel 1	Channel 2	Period
Delay: 0 ps	Doub: 10.0 ns	20 ns
Width: 3.5 ns	Width: 3.5 ns	
High: -0.9 V	High: -0.9 V	
Low: -1.7 V	Low: -1.7 V	

b Enable the pulse generator channel 2 COMP (with the LED on).

3 Set up the oscilloscope.

Oscilloscope Setup

Time Base	**Display**	**Delta V**	**Delta t**
Time/Div: 1.00 ns/div	avg	V markers on	T markers on
	# of avg: 16	marker 1 position: Chan 1	start on: Pos Edge 1
	screen: dual	marker 2 position: Chan 1	stop on: Neg Edge 1

Channel

	Channel 1	**Channel 2**
Display	on	on
Probe Atten	20.00	20.00
Offset	–1.3 V	–1.3 V
Volts/Div	400 mV	400 mV

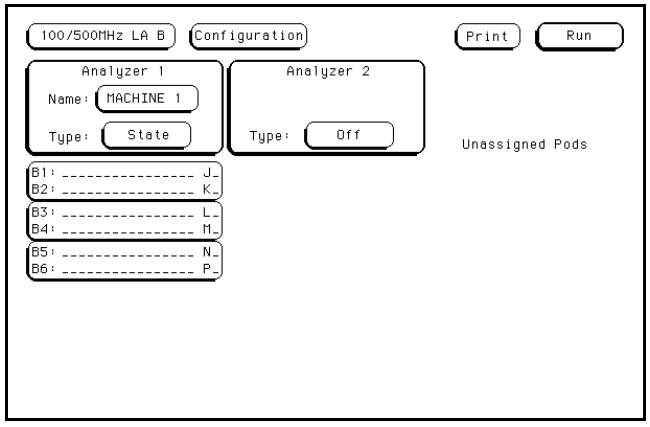
Set up the logic analyzer

1 Set up the Configuration menu.

a In the System Configuration menu, touch System, then select 100/500 MHz.

b In the Configuration menu, assign all pods to Machine 1. To assign the pods, touch the pod fields, then select Machine 1.

c In the Analyzer 1 box, touch the Type field, then select State.

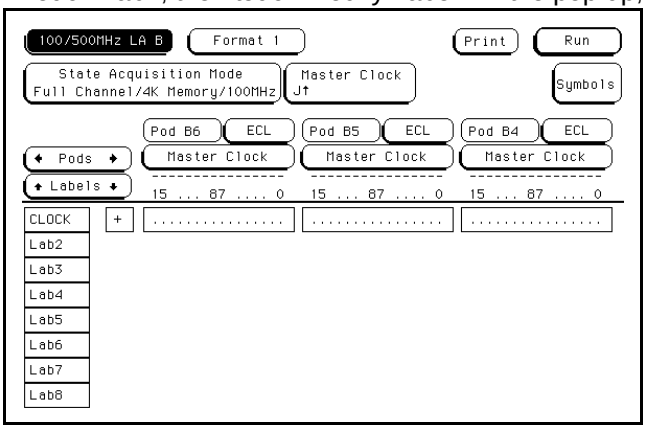


2 Set up the Format menu.

a Touch Configuration, then select Format. In the Format menu, touch State Acquisition Mode, then select Full Channel/4K Memory/100MHz.

b Touch the field to the right of each Pod field, then select ECL. The screen does not show all Pod fields at one time. To access more Pod fields, turn the knob.

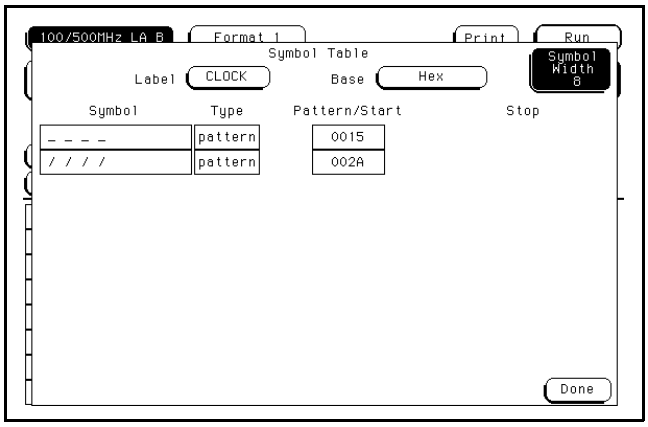
c Touch Lab1, then touch Modify Label. In the pop-up, type clock, then touch Done.



3 Set up the Symbols menu.

a Touch Symbols, then touch New symbol. In the pop-up, type "_ _ _ _," then touch Done. Touch the Pattern/Start field. In the pop-up menu, type "0015," then touch done.

b Touch the Symbol field, then select Add a Symbol. In the pop-up, type "////," then touch Done. Touch the Pattern/Start field on the same line as the "////" Symbols. In the pop-up menu, type "002A," then touch Done. Touch Done to exit Symbols.



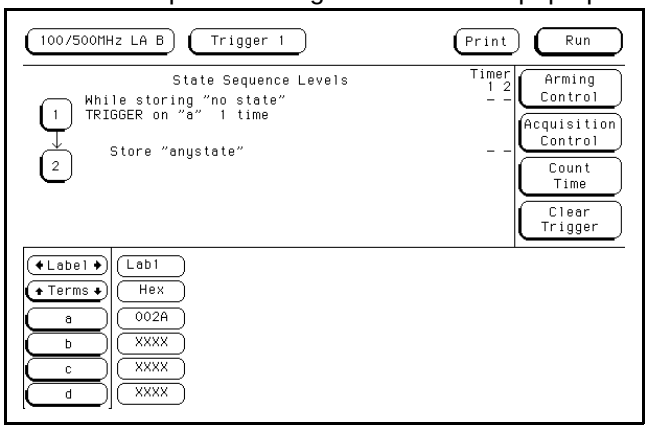
4 Set up the Trigger menu.

a Touch Format, then select Trigger. In the Trigger menu, touch Clear Trigger, then select All.

b Touch the Count field, then touch off. In the pop-up, select Time. Touch Done to exit the Count menu.

c Touch the field labeled 1 under the State Sequence Levels. Touch the field labeled "anystate," then select "no state."

d Touch the pattern recognizer "a." In the pop-up menu, type "002A," then touch Done.



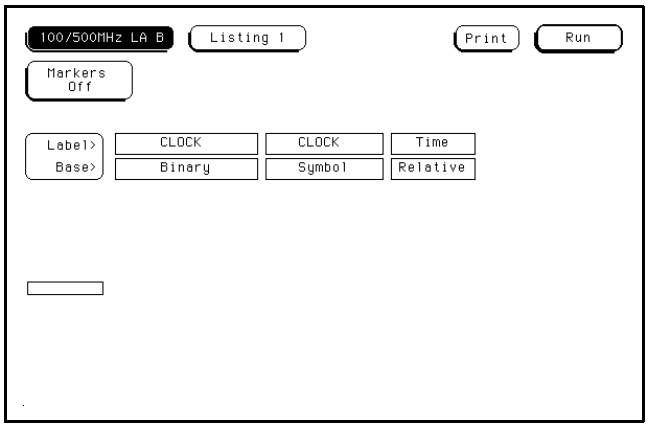
5 Set up the Listing menu.

a Touch Trigger, then select Listing.

b Touch the Clock base field, then select Binary.

c Touch the Clock label field, select Insert, then select Clock.

d Touch the base field below the second Clock label, then select Symbol.



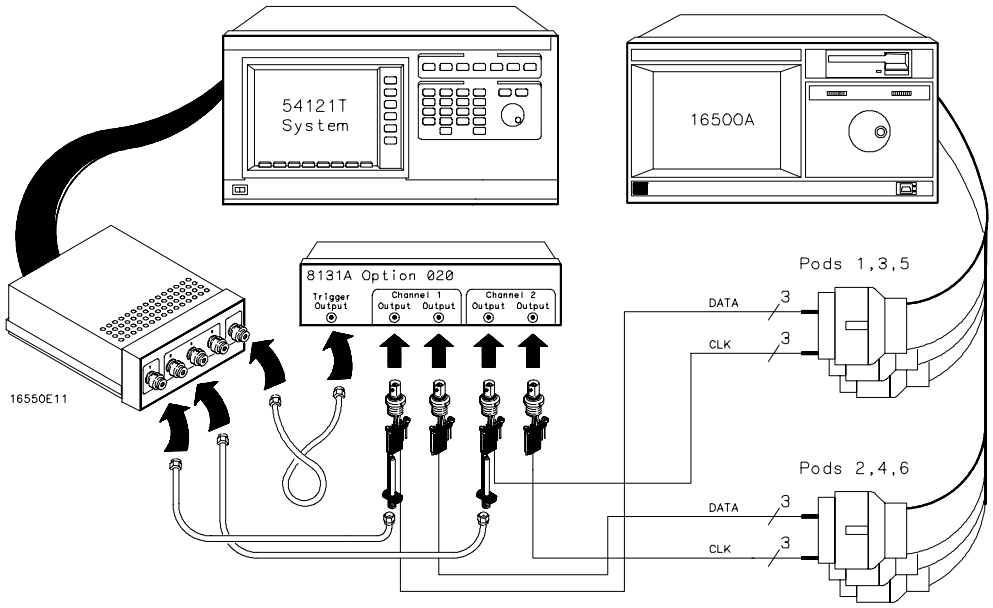
Connect the logic analyzer

1 Using the 6-by-2 test connectors, connect the first combination of logic analyzer clock and data channels listed the table below to the pulse generator.

2 Using SMA cables, connect channel 1, channel 2, and trigger from the oscilloscope to the pulse generator.

Connect the Logic Analyzer to the Pulse Generator

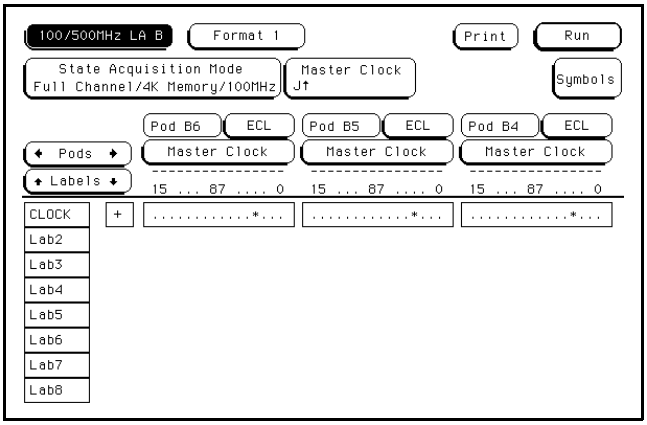
Testing Combinations	Connect to HP 8131A Channel 1 Output	Connect to HP 8131A Channel 1 Output	Connect to HP 8131A Channel 2 Output	Connect to HP 8131A Channel 2 Output
1	Pod 1, channel 3 Pod 3, channel 3 Pod 5, channel 3	Pod 2, channel 3 Pod 4, channel 3 Pod 6, channel 3	J-clock L-clock N-clock	K-clock M-clock P-clock
2	Pod 1, channel 11 Pod 3, channel 11 Pod 5, channel 11	Pod 2, channel 11 Pod 4, channel 11 Pod 6, channel 11	J-clock L-clock N-clock	K-clock M-clock P-clock



3 Activate the data channels that are connected according to the table on the previous page.

a Touch Listing, then select Format.

b Touch the field showing the channel assignments for one of the pods being tested. In the pop-up menu, touch clear. Using the knob, move the cursor to the data channels to be tested. Touch the asterisk field to put asterisks in the channel positions, activating the channels, then touch Done. Follow this step for the remaining five pods.



Check the clock pulse width

Using the oscilloscope, verify that the clock pulse width is 3.450 ns, +50 ps or –100 ps.

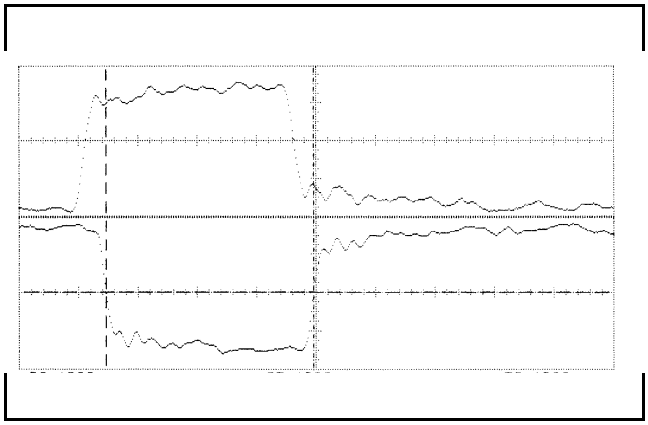
1 Enable the pulse generator channel 1 and channel 2 outputs.

2 In the oscilloscope Timebase menu, select Delay. Using the oscilloscope knob, position the clock waveform so that the waveform is centered on the screen.

3 In the oscilloscope Delta V menu, select Marker 1 Position Chan 2, Marker 1 at –1.3000 V. Select Marker 2 Position Chan 2, Marker 2 at –1.3000 V.

4 In the oscilloscope Delta t menu, select Start On Neg Edge 1. Select Stop on Pos Edge 1.

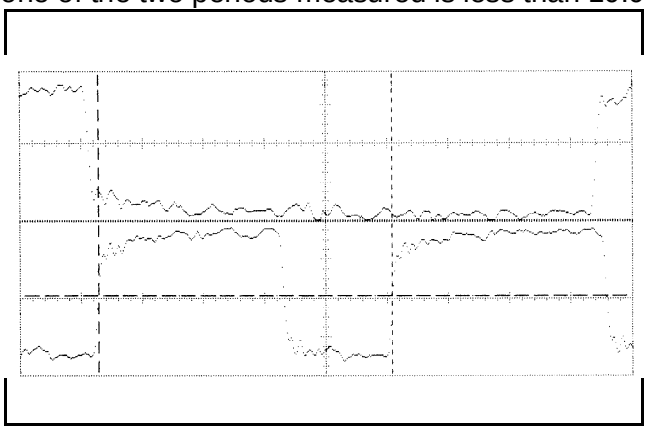
5 If the pulse width is outside the limits, adjust the pulse generator channel 2 width and select the oscilloscope Precision Edge Find until the pulse width is within limits.



Check the clock period

Using the oscilloscope, verify that the clock period is 10 ns.

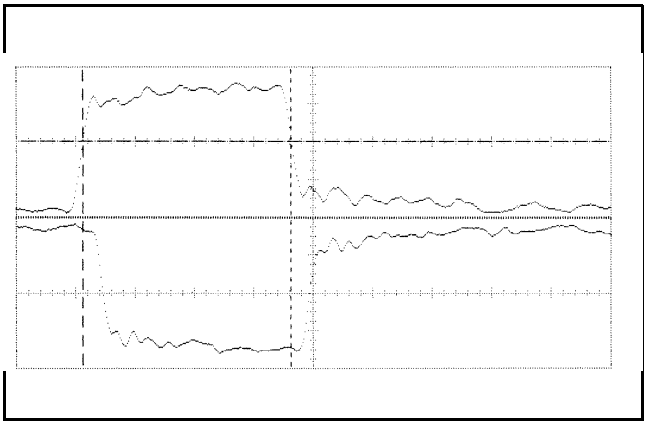
1. In the oscilloscope Timebase menu, select Sweep Speed 2.00 ns/div.
2. Select Delay. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.
3. In the oscilloscope Measure menu, select Measure Chan 2, then select Period. If the period is not less than 10.000 ns, go to step 4. If the period is less than 10.000 ns, go to the next page.
4. In the oscilloscope Timebase menu, add 10 ns to the delay.
5. In the oscilloscope Measure menu, select Period. If the period is not less than 10.000 ns, decrease the pulse generator Chan 2 Doub in 10-ps increments until one of the two periods measured is less than 10.000 ns.



Check the data pulse width

Using the oscilloscope, verify that the data pulse width is 3.450 ns, +50 ps or -100 ps.

1. In the oscilloscope Timebase menu, select Sweep Speed 1.00 ns/div.
2. Select Delay. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.
3. In the oscilloscope Delta V menu, select Marker 1 Position Chan 1, Marker 1 at –1.3000 V. Select Marker 2 position Chan 1, marker 2 at –1.3000 V.
4. In the oscilloscope Delta t menu, select Start On Pos Edge 1. Select Stop on Neg Edge 1.
5. Select Precision Edge Find.
6. If the pulse width is outside the limits, adjust the pulse generator channel 1 width



and select the oscilloscope Precision Edge Find until the pulse width is within limits.

Check the setup/hold combination

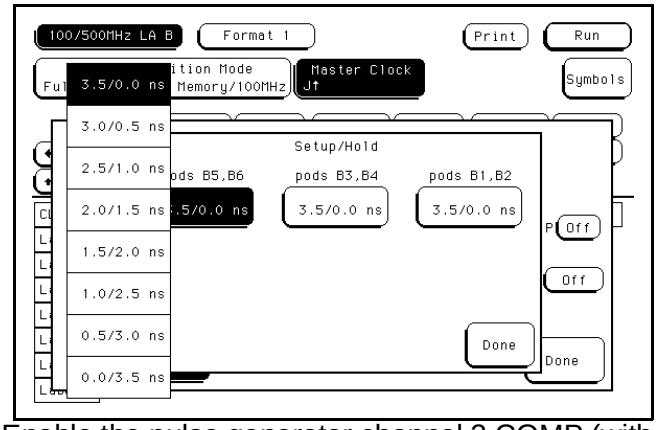
1 Select the logic analyzer setup/hold time.

a In the logic analyzer Format menu, touch Master Clock.

b Touch the Setup/Hold field and select the setup/hold combination to be tested for all pods. The first time through this test, select the top combination in the following table.

Setup/Hold Combinations
3.5/0.0 ns
0.0/3.5 ns
1.5/2.0 ns

c Touch Done to exit the setup/hold combinations.



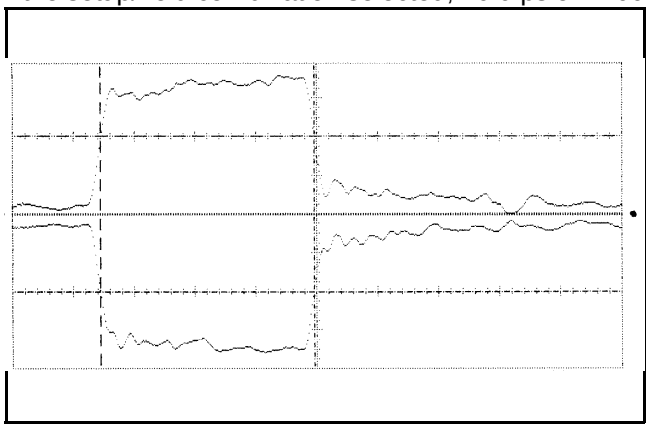
2 Enable the pulse generator channel 2 COMP (with the LED on).

3 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or –100 ps.

a In the oscilloscope Delta V menu, select Marker 1 Position Chan 1, Marker 1 at –1.3000 V. Select Marker 2 Position Chan 2, Marker 2 at –1.3000 V.

b In the oscilloscope Delta t menu, select Start on Pos Edge 1. Select Stop on Pos Edge 1.

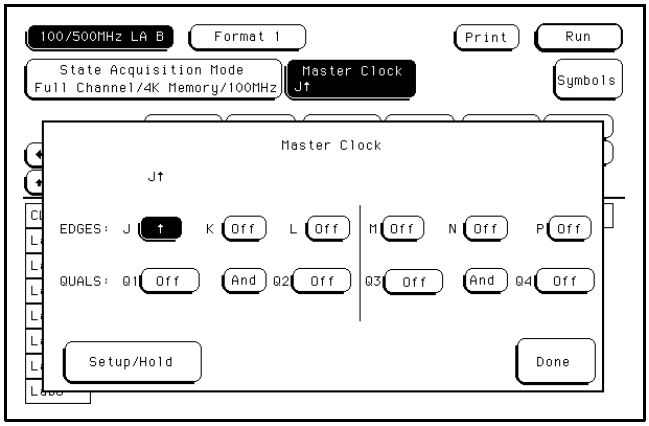
c Adjust the pulse generator channel 1 Delay and select Precision Edge Find in the oscilloscope Delta t menu until the pulses are aligned according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps.



4 Select the clock to be tested.

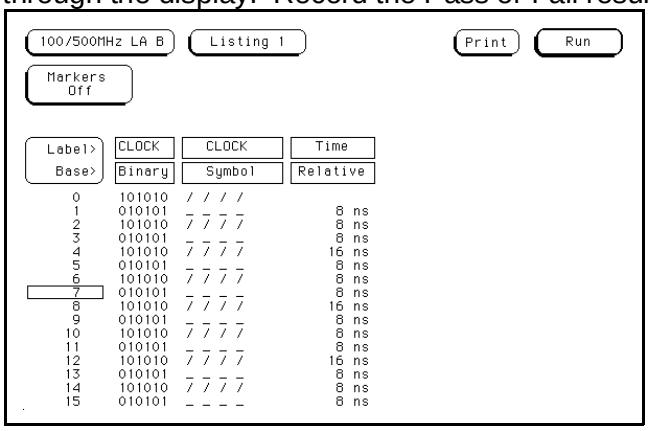
a In the Master Clock menu, touch the clock field to be tested and then select the clock edge as indicated in the table. The first time through this test, select the top clock and edge.

Clocks
J↑
K↓
L↑
M↓
N↑
P↓



b Touch Done to exit the Master Clock menu.

5 In the logic analyzer Format menu, touch Run. The display should show a checkerboard pattern of alternating 1s and 0s, and the symbols column should show alternating lines of "_ _ _ _" and "/ / / /." Verify the pattern by scrolling through the display. Record the Pass or Fail results in the performance test record.



6 Test the next clock.

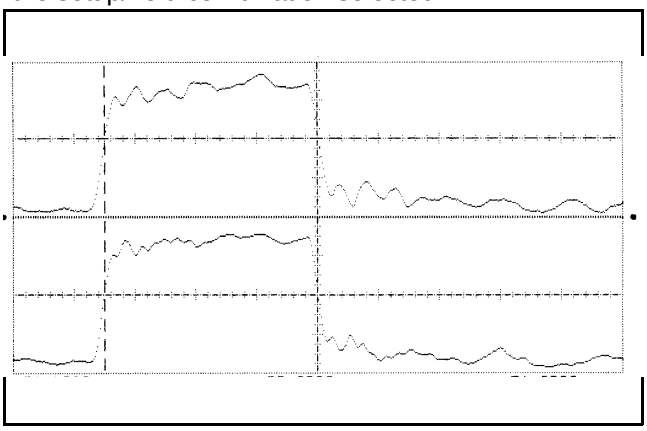
- **a** In the logic analyzer Format menu, touch Master Clock.
- **b** Turn off the clock just tested.
- **c** Repeat steps 4, 5, and 6 for the next clock edge listed in the table in step 4, until all listed clock edges have been tested.

7 Disable the pulse generator channel 2 COMP (with the LED off).

8 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or –100 ps.

- **a** In the oscilloscope Delta V menu, select Marker 1 Position Chan 1, Marker 1 at –1.3000 V. Select Marker 2 Position Chan 2, Marker 2 at –1.3000 V.
- **b** In the oscilloscope Delta t menu, select Start on Pos Edge 1. Select Stop on Neg Edge 1.

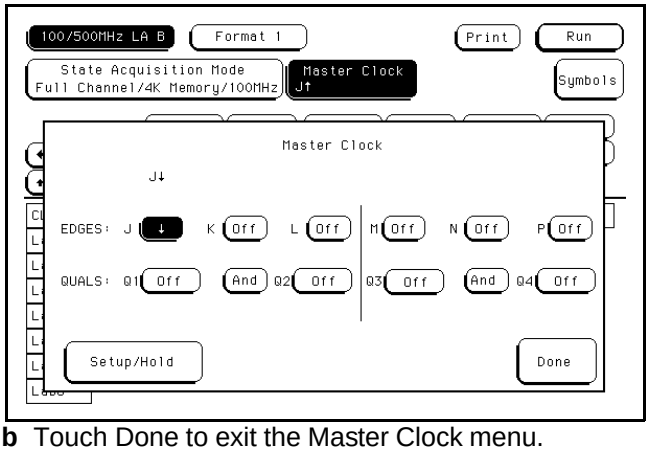
c Adjust the pulse generator channel 1 Delay and select Precision Edge Find in the oscilloscope Delta t menu until the pulses are aligned according to the setup time of the setup/hold combination selected.



9 Select the clock to be tested.

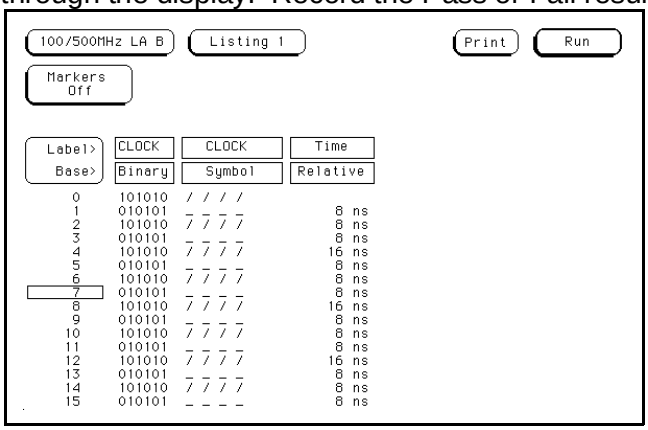
a In the Master Clock menu, touch the clock field to be tested and then select the clock edge as indicated in the table. The first time through this test, select the top clock and edge.

Clocks
J↓
K↑
L↓
M↑
N↓
P↑



b Touch Done to exit the Master Clock menu.

10 In the logic analyzer Format menu, touch Run. The display should show a checkerboard pattern of alternating 1s and 0s, and the symbols column should show alternating lines of "_ _ _ _" and "/ / / /." Verify the pattern by scrolling through the display. Record the Pass or Fail results in the performance test record.



11 Test the next clock.

- **a** In the logic analyzer Format menu, touch Master Clock.
- **b** Turn off the clock just tested.
- **c** Repeat steps 9, 10, and 11 for the next clock edge listed in the table in step 9, until all listed clock edges have been tested.

12 Test the next setup/hold combination.

- **a** In the logic analyzer Format menu, touch Master Clock.
- **b** Turn off the clock just tested.
- **c** Repeat steps 1 through 12 for the next setup/hold combination listed in step 1 on page 3–30, until all listed setup/hold combinations have been tested.

When aligning the data and clock waveforms using the oscilloscope, align the waveforms according to the setup time of the setup/hold combination being tested, +0.0 ps or –100 ps.

Test the next channels

- Connect the next combination of data channels and clock channels, then test them.

  Start on page 3–26, "Connect the logic analyzer," connect the next combination, then continue through the complete test.

To test the multiple-clock, multiple-edge, state acquisition

Testing the multiple-clock, multiple-edge, state acquisition verifies the performance of the following specifications:

- Minimum master to master clock time.
- Maximum state acquisition speed.
- Setup/Hold time.
- Minimum clock pulse width.

Two-card modules must be reconfigured as one-card modules for this test.

This test checks two combinations of data using multiple clocks at three selected setup/hold times.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	100 MHz 3.5 ns pulse width, <600 ps rise time	HP 8131A option 020
Digitizing Oscilloscope	≥ 6 GHz bandwidth, <58 ps rise time	HP 54121T
Adapter	SMA(m)-BNC(f)	HP 1250-1200
SMA Coax Cable (Qty 3)		HP 8120-4948
Coupler	BNC(m-m)	HP 1250-0216
BNC Test Connector, 6x2 (Qty 4)		

Set up the equipment

1 Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes before beginning the test if you have not already done so.

2 Set up the pulse generator.

a Set up the pulse generator according to the following table.

Pulse Generator Setup

Channel 1	Channel 2	Period
Delay: 0 ps	Doub: 10.0 ns	20 ns
Width: 4.5 ns	Width: 3.5 ns	
High: –0.9 V	High: –0.9 V	
Low: –1.7 V	Low: –1.7 V	

b Enable the pulse generator channel 2 COMP (with the LED on).

3 Set up the oscilloscope.

Oscilloscope Setup

Time Base	**Display**	**Delta V**	**Delta t**
Time/Div: 1.00 ns/div	avg	V markers on	T markers on
	# of avg: 16	marker 1 position: Chan 1	start on: Pos Edge 1
	screen: dual	marker 2 position: Chan 1	stop on: Neg Edge 1

Channel

	Channel 1	**Channel 2**
Display	on	on
Probe Atten	20.00	20.00
Offset	–1.3 V	–1.3 V
Volts/Div	400 mV	400 mV

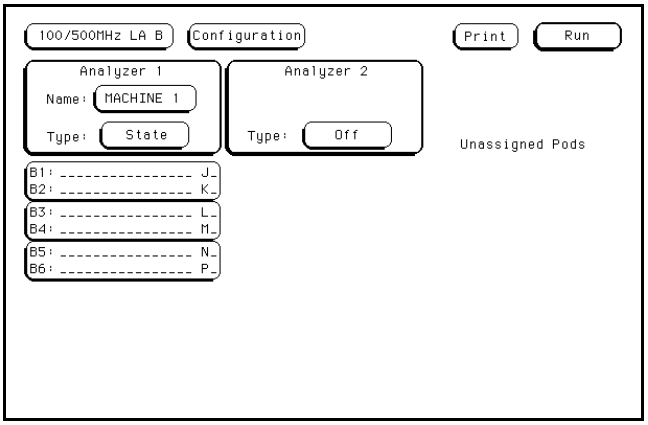
Set up the logic analyzer

1 Set up the Configuration menu.

a In the System Configuration menu, touch System, then select 100/500 MHz LA.

b In the Configuration menu, assign all pods to Machine 1. To assign all pods, touch the pod fields, then select Machine 1.

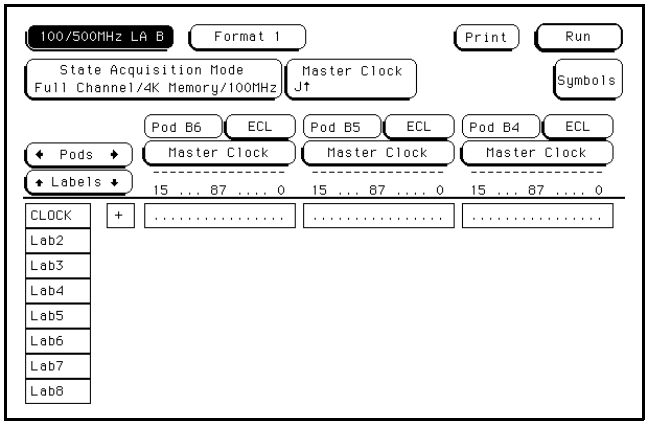
c In the Analyzer 1 box, touch the Type field, then select State.



2 Set up the Format menu.

a Touch Configuration, then select Format. In the Format menu, touch State Acquisition Mode, then select Full Channel/4K Memory/100MHz.

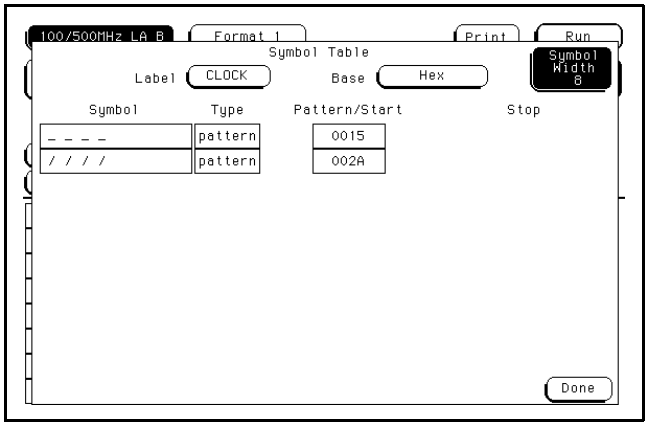
b Touch the field to the right of each Pod field, then select ECL. The screen does not show all Pod fields at one time. To access more Pod fields, turn the knob.



3 Set up the Symbols menu.

a Touch Symbols, then touch New symbol. In the pop up, type "_ _ _ _," then touch Done. Touch the Pattern/Start field. In the pop up menu, type "0015," then touch Done.

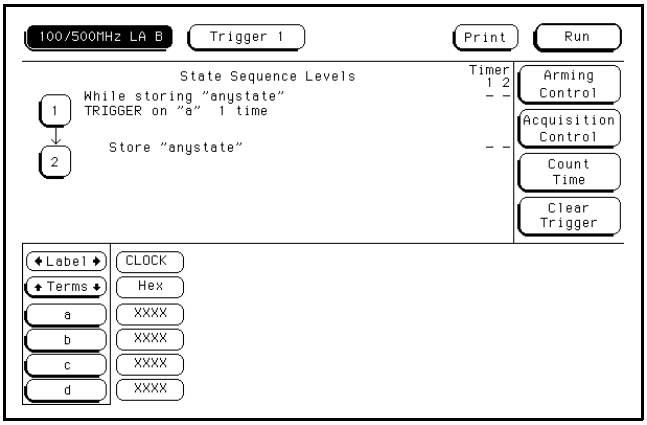
b Touch the Symbol field, then select Add a Symbol. In the pop up, type "/ / / /," then touch Done. Touch the Pattern/Start field on the same line as the "/ / / /" symbol. In the pop up menu, type "002A," then touch Done. Touch Done to exit Symbols.



4 Set up the Trigger menu.

a Touch Format, then select Trigger. In the Trigger menu, touch Clear Trigger, then select All.

b Touch the Count Off field. In the Count menu, touch Off. In the pop-up, select Time, then touch Done to exit.



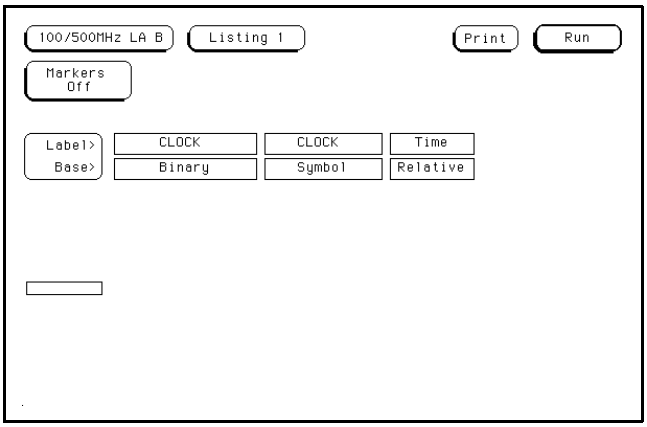
5 Set up the Listing menu.

a Touch Trigger, then select Listing.

b Touch the Clock base field, then select Binary.

c Touch the Clock label field, then select Insert. In the pop-up, select Clock.

d Touch the base field below the second Clock label, then select Symbol.

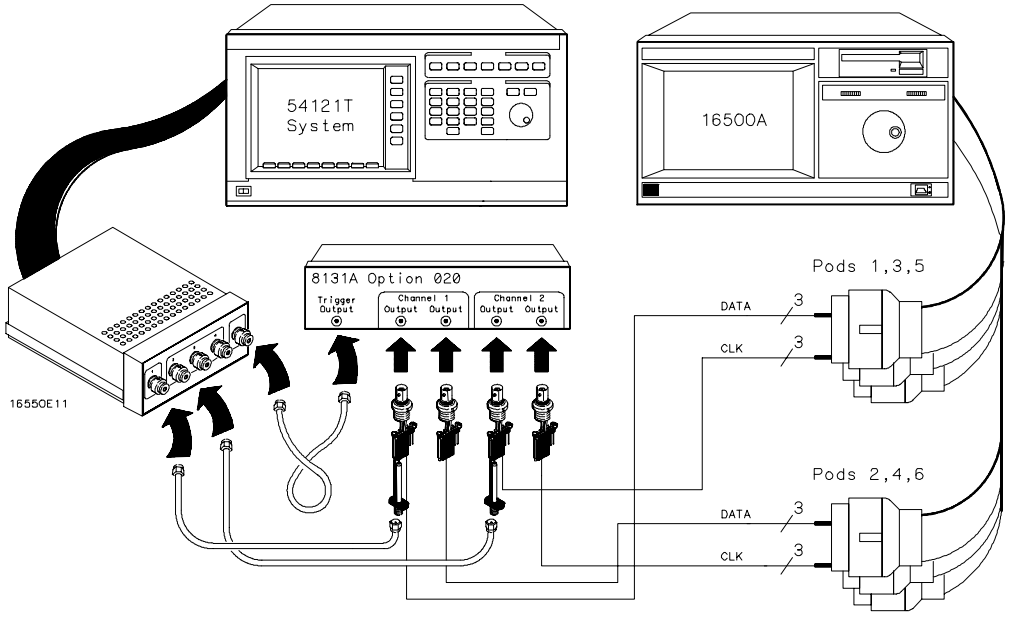


Connect the logic analyzer

1. Using the 6-by-2 test connectors, connect the first combination of logic analyzer clock and data channels listed in the table below to the pulse generator.
2. Using SMA cables, connect channel 1, channel 2, and trigger of the oscilloscope to the pulse generator.

Connect the Logic Analyzer to the Pulse Generator

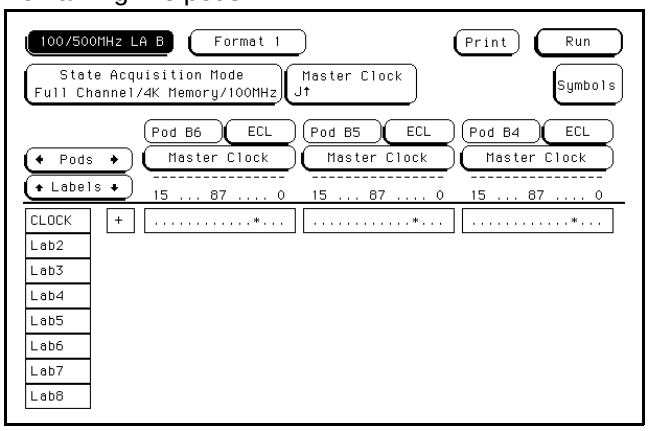
Testing Combinations	Connect to HP 8131A Channel 1 Output	Connect to HP 8131A Channel 1 Output	Connect to HP 8131A Channel 2 Output	Connect to HP 8131A Channel 2 Output
1	Pod 1, channel 3 Pod 3, channel 3 Pod 5, channel 3	Pod 2, channel 3 Pod 4, channel 3 Pod 6, channel 3	J-clock L-clock N-clock	K-clock M-clock P-clock
2	Pod 1, channel 11 Pod 3, channel 11 Pod 5, channel 11	Pod 2, channel 11 Pod 4, channel 11 Pod 6, channel 11	J-clock L-clock N-clock	K-clock M-clock P-clock



3 Activate the data channels that are connected according to the table on the previous page.

a Touch Listing, then select Format.

b Touch the field showing the channel assignments for one of the pods being tested. In the pop-up menu, touch clear. Using the knob, move the cursor to the data channels to be tested. Touch the asterisk field to put asterisks in the channel positions, activating the channels, then touch Done. Follow this step for the remaining five pods.



Check the clock pulse width

Using the oscilloscope, verify that the clock pulse width is 3.450 ns, +50 ps or –100 ps.

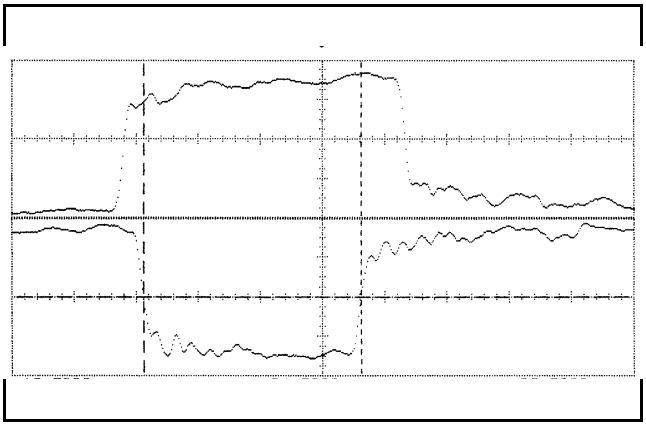
1 Enable the pulse generator channel 1 and channel 2 outputs (with the LED off).

2 In the oscilloscope Timebase menu, select Delay. Using the oscilloscope knob, position the clock waveform so that the waveform is centered on the screen.

3 In the oscilloscope Delta V menu, select Marker 1 Position Chan 2, Marker 1 at –1.3000 V. Select Marker 2 Position Chan 2, Marker 2 at –1.3000 V.

4 In the oscilloscope Delta t menu, select Start On Neg Edge 1. Select Stop On Pos Edge 1.

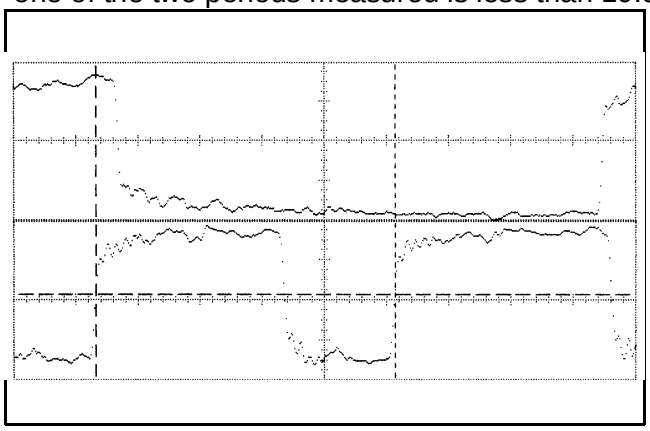
5 If the pulse width is outside of the limits, adjust the pulse generator channel 2 width and select the oscilloscope Precision Edge Find until the pulse width is within limits.



Check the clock period

Using the oscilloscope verify that the clock period is 10 ns.

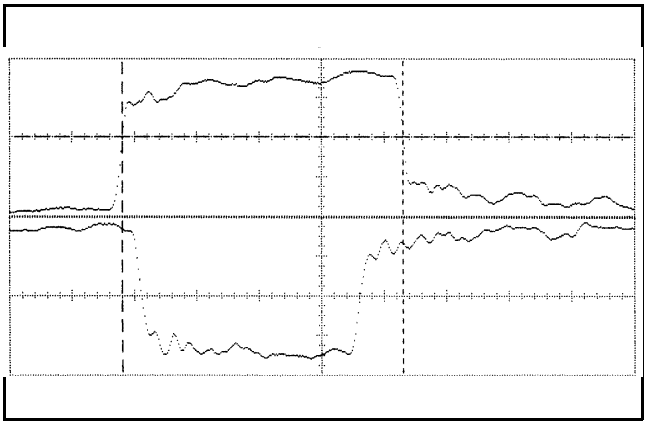
1. In the oscilloscope Timebase menu, select Sweep Speed 2.00 ns/div.
2. Select Delay. Using the oscilloscope knob position the clock waveform so that a rising edge appears at the left of the display.
3. In the oscilloscope Measure menu, select Measure Chan 2, then select Period. If the period is not less than 10.000 ns, go to step 4. If the period is less than 10.000 ns, go to the next page.
4. In the oscilloscope Timebase menu, add 10 ns to the Delay.
5. In the oscilloscope Measure menu, select Period. If the period is not less than 10.000 ns, decrease the pulse generator Chan 2 DOUB in 10 ps increments until one of the two periods measured is less than 10.000 ns.



Check the data pulse width

Using the oscilloscope verify that the data pulse width is 4.450 ns, +50 ps or –100 ps.

1. In the oscilloscope Timebase menu, select Sweep Speed 1.00 ns/div.
2. Select Delay. Using the oscilloscope knob, position the data waveform so that the waveform is centered in the screen.
3. In the oscilloscope Delta V menu, select Marker 1 Position Chan 1, Marker 1 at –1.3000 V. Select Marker 2 Position Chan 1, Marker 2 at –1.3000 V.
4. In the oscilloscope Delta t menu, select Start On Pos Edge 1. Select Stop on Neg Edge 1.
5. If the pulse width is outside of the limits adjust the pulse generator channel 1 width



and select the oscilloscope Precision Edge Find until the pulse width is within limits.

Check the setup/hold with single clock edges, multiple clocks

1 Select the logic analyzer setup/hold time.

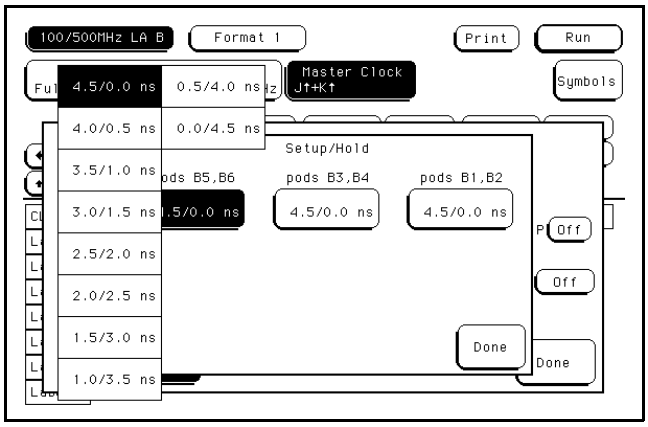
a In the logic analyzer Format menu, touch Master Clock.

b Select and activate any two clock edges.

c Touch the Setup/Hold field and select the setup/hold to be tested for all pods. The first time through this test, select the top combination in the following table.

Setup/Hold Combinations
4.5/0.0 ns
0.0/4.5 ns
2.0/2.5 ns

d Touch Done to exit the setup/hold combinations.



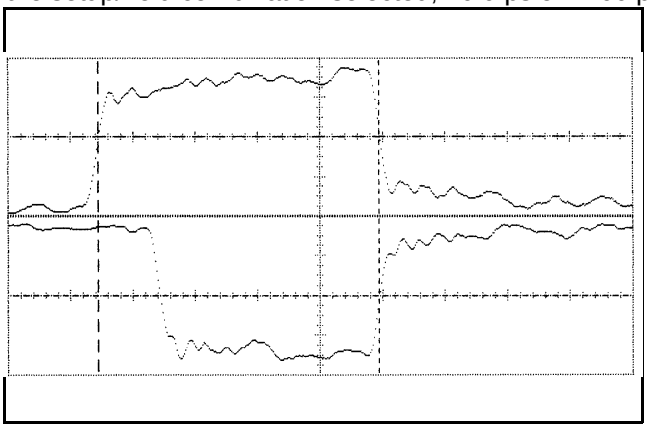
2 Enable the pulse generator channel 2 COMP (with the LED on).

3 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps.

a In the oscilloscope Delta V menu, select Marker 1 Position Chan 1, Marker 1 at –1.3000 V. Select Marker 2 Position Chan 2, Marker 2 at –1.3000 V.

b In the oscilloscope Delta t menu, select Start on Pos Edge 1. Select Stop on Pos Edge 1.

c Adjust the pulse generator channel 1 Delay and select Precision Edge Find in the oscilloscope Delta t menu until the pulses are aligned according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps.

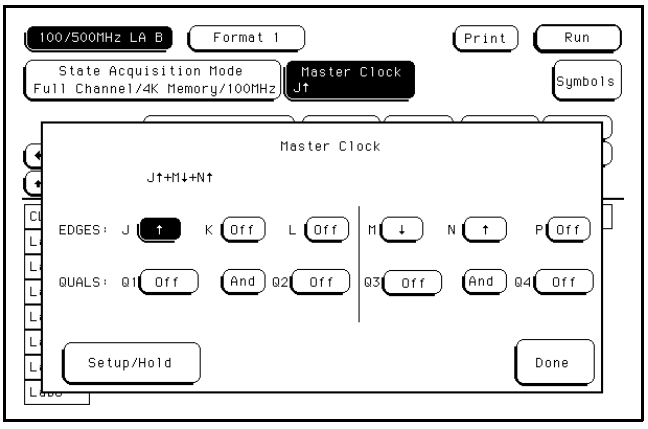


4 Select the clocks to be tested.

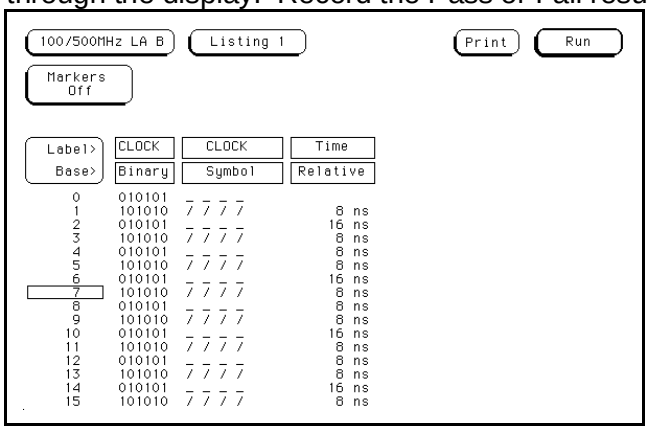
a Touch the clock field to be tested and then select the clock edges as indicated in the table. The first time through this test, select the top clocks and edges.

Clocks
J↑ + M↓ + N↑
K↓ + L↑ + P↓

b Touch Done to exit the Master Clock menu.



5 In the logic analyzer Format menu, touch Run. The display should show a checkerboard pattern of alternating 1s and 0s, and the symbols column should show alternating lines of "_ _ _ _" and "/ / / /." Verify the pattern by scrolling through the display. Record the Pass or Fail results in the performance test record.



6 Test the next clocks.

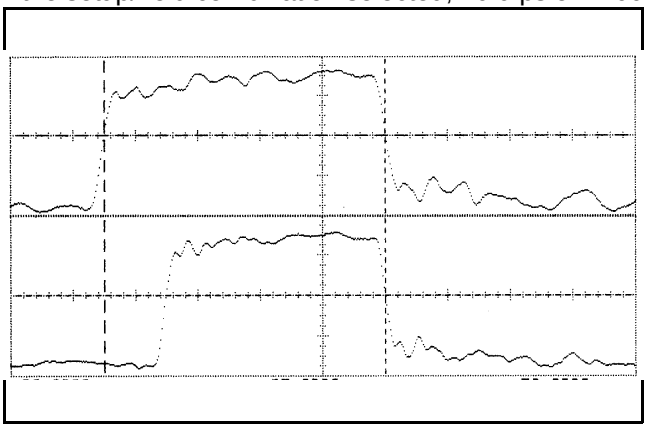
- **a** In the logic analyzer Format menu, touch Master Clock.
- **b** Turn off the clocks just tested.
- **c** Repeat steps 4, 5, and 6 for the next clock edge listed in the table in step 4, until all listed clock edges have been tested.

7 Disable the pulse generator channel 2 COMP (with the LED off).

8 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps.

- **a** In the oscilloscope Delta V menu, select Marker 1 Position Chan 1, Marker 1 at –1.3000 V. Select Marker 2 Position Chan 2, Marker 2 at –1.3000 V.
- **b** In the oscilloscope Delta t menu, select Start On Pos Edge 1. Select Stop on Neg Edge 1.

c Adjust the pulse generator channel 1 Delay and select Precision Edge Find in the oscilloscope Delta t menu until the pulses are aligned according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps.

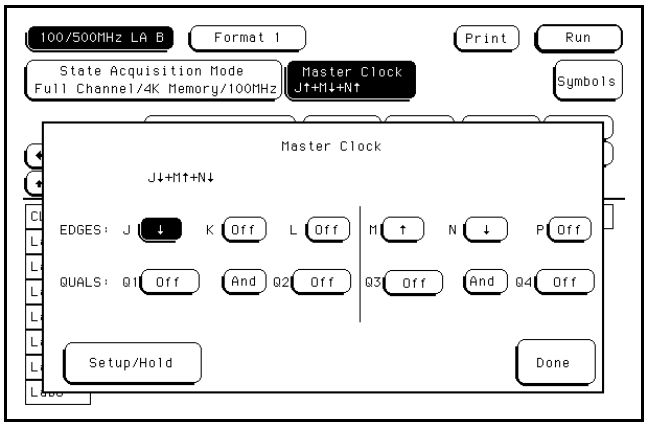


9 Select the clocks to be tested.

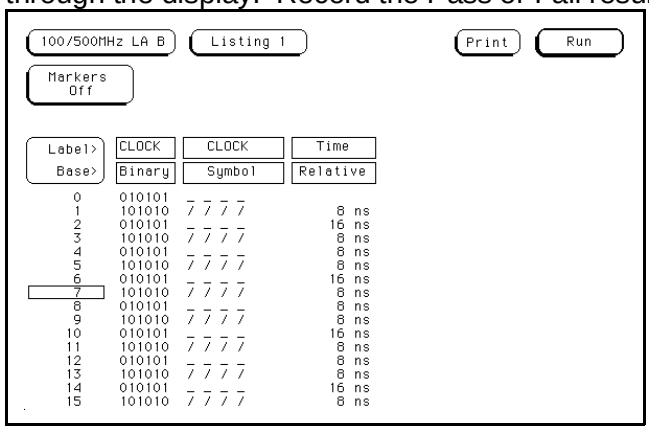
a Touch the clock field to be tested and then select the clock edges as indicated in the table. The first time through this test, select the top clocks and edges.

Clocks
J↓ + M↑ + N↓
K↑ + L↓ + P↑

b Touch Done to exit the Master Clock menu.



10 In the logic analyzer Format menu, touch Run. The display should show a checkerboard pattern of alternating 1s and 0s, and the symbols column should show alternating lines of "_ _ _ _" and "/ / / /." Verify the pattern by scrolling through the display. Record the Pass or Fail results in the performance test record.



11 Test the next clocks.

- **a** In the logic analyzer Format menu, touch Master Clock.
- **b** Turn off the clocks just tested.
- **c** Repeat steps 9, 10, and 11 for the next clock edges listed in the table in step 9, until all listed clock edges have been tested.

12 Test the next setup/hold combination.

- **a** In the logic analyzer Format menu, touch Master Clock.
- **b** Turn off the clocks just tested.
- **c** Repeat steps 1 through 12 for the next setup/hold combination listed in step 1 on page 3-43, until all listed setup/hold combinations have been tested.

When aligning the data and clock waveforms using the oscilloscope, align the waveforms according to the setup time of the setup/hold combination being tested, +0.0 ps or –100 ps.

Test the next channels

- Connect the next combination of data channels and clock channels, then test them.

  Start on page 3–39 "Connect the logic analyzer," connect the next combination, then continue through the complete test.

To test the single-clock, multiple-edge, state acquisition

Testing the single-clock, multiple-edge, state acquisition verifies the performance of the following specifications:

- Minimum master to master clock time.
- Maximum state acquisition speed.
- Setup/Hold time.
- Minimum clock pulse width.

Two-card modules must be reconfigured as one-card modules for this test.

This test checks two combinations of data using a multiple-edge single clock at three selected setup/hold times.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	100 MHz 3.5 ns pulse width, <600 ps rise time	HP 8131A option 020
Digitizing Oscilloscope	≥ 6 GHz bandwidth, <58 ps rise time	HP 54121T
Adapter	SMA(m)-BNC(f)	HP 1250-1200
SMA Coax Cable (Qty 3)		HP 8120-4948
Coupler	BNC(m-m)	HP 1250-0216
BNC Test Connector, 6x2 (Qty 4)		

Set up the equipment

1 Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes before beginning the test if you have not already done so.

2 Set up the pulse generator according to the following table.

Pulse Generator Setup

Channel 1	Channel 2	Period
Doub: 10 ns	Delay: 0 ps	20 ns
Width: 4.0 ns	Dcyc: 50%	
High: –0.9 V	High: –0.9 V	
Low: –1.7 V	Low: –1.7 V	
COMP: Disabled (LED off)	COMP: Disabled (LED off)	

3 Set up the oscilloscope.

Oscilloscope Setup

Time Base	**Display**	**Delta V**	**Delta t**
Time/Div: 1.00 ns/div	avg	V markers on	T markers on
	# of avg: 16	marker 1 position: Chan 1	start on: Neg Edge 1
	screen: dual	marker 2 position: Chan 1	stop on: Neg Edge 2

Channel

	Channel 1	**Channel 2**
Display	on	on
Probe Atten	20.00	20.00
Offset	–1.3 V	–1.3 V
Volts/Div	400 mV	400 mV

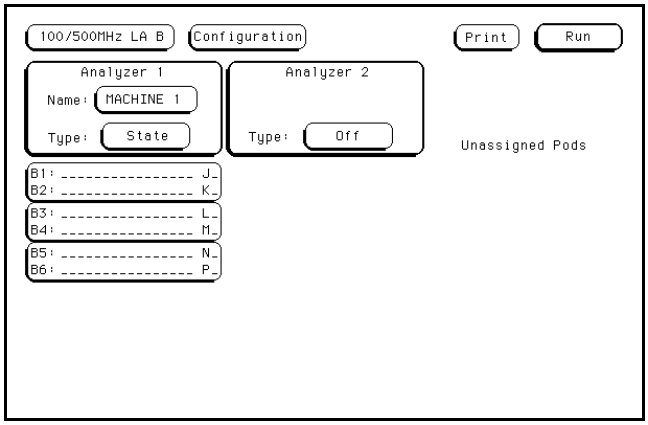
Set up the logic analyzer

1 Set up the Configuration menu.

a In the System Configuration menu, touch System, then select 100/500 MHz LA.

b In the Configuration menu, assign all pods to Machine 1. To assign all pods, touch the pod fields, then select Machine 1.

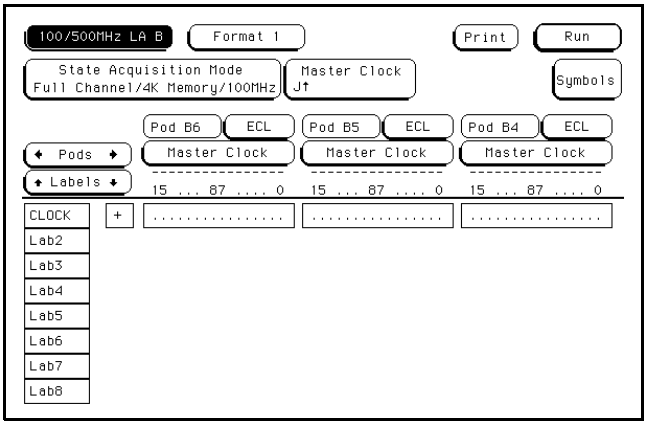
c In the Analyzer 1 box, touch the Type field, then select State.



2 Set up the Format menu.

a Touch Configuration, then select Format. In the Format menu, touch State Acquisition Mode, then select Full Channel/4K Memory/100MHz.

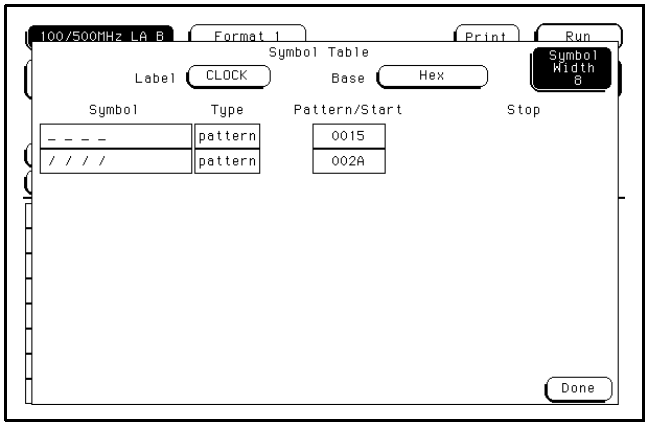
b Touch the field to the right of each Pod field, then select ECL. The screen does not show all Pod fields at one time. To access more Pod fields, turn the knob.



3 Set up the Symbols menu.

a Touch Symbols, then touch New symbol. In the pop up, type "_ _ _ _," then touch Done. Touch the Pattern/Start field. In the pop-up menu, type "0015," then touch Done.

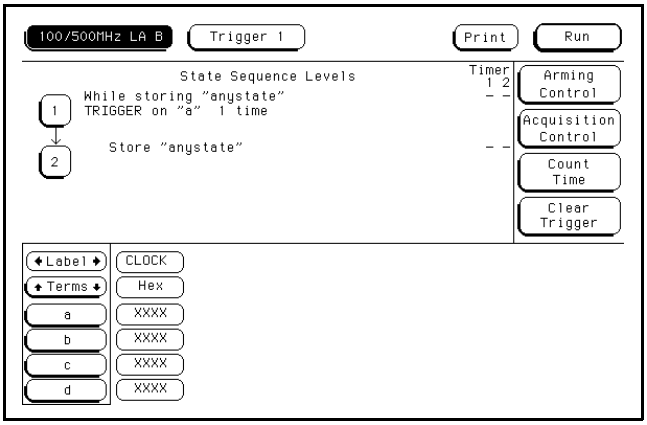
b Touch the Symbol field, then select Add a Symbol. In the pop-up, type "/ / / /," then touch Done. Touch the Pattern/Start field on the same line as the "/ / / /" symbol. In the pop-up menu, type "002A," then touch Done. Touch Done to exit Symbols.



4 Set up the Trigger menu.

a Touch Format, then select Trigger. In the Trigger menu, touch Clear Trigger, then select All.

b Touch the Count Off field. In the Count menu, touch Off. In the pop-up, select Time, then touch Done to exit.



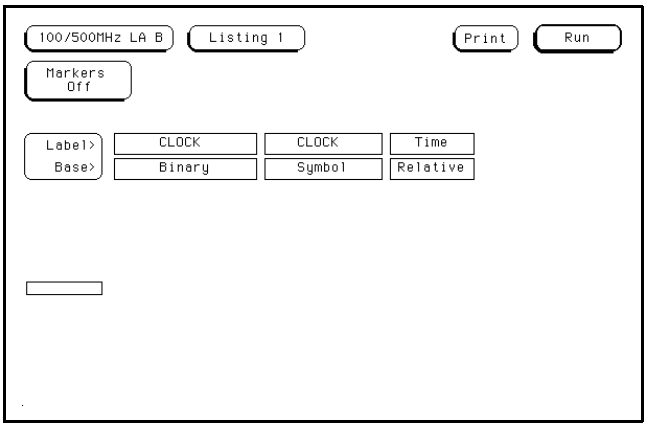
5 Set up the Listing menu.

a Touch Trigger, then select Listing.

b Touch the Clock base field, then select Binary.

c Touch the Clock label field, then select Insert. In the pop up, select Clock.

d Touch the base field below the second Clock label, then select Symbol.

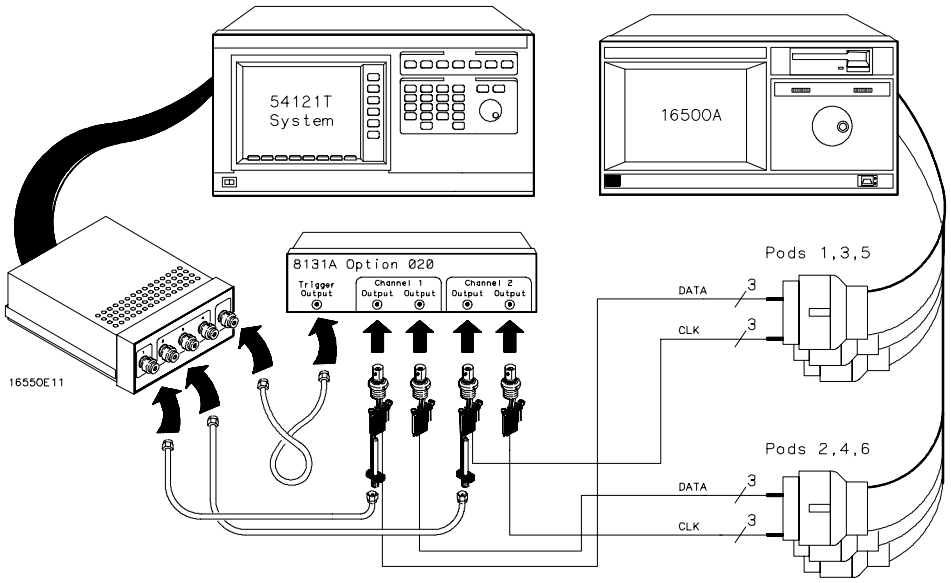


Connect the logic analyzer

1. Using the 6-by-2 test connectors, connect the first combination of logic analyzer clock and data channels listed in the table below to the pulse generator.
2. Using the SMA cables, connect channel 1, channel 2, and trigger from the oscilloscope to the pulse generator.

Connect the Logic Analyzer to the Pulse Generator

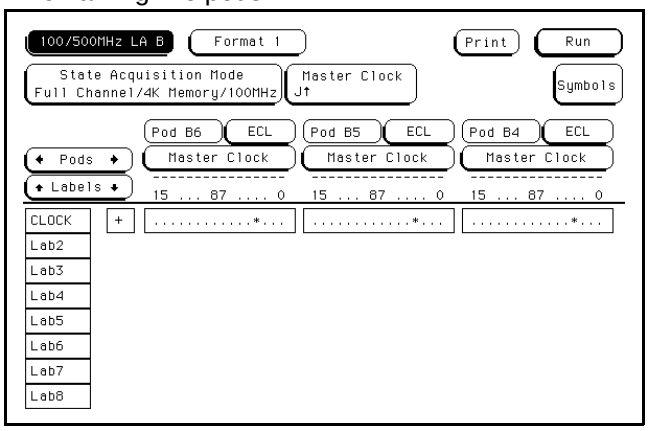
Testing Combinations	Connect to HP 8131A Channel 1 Output	Connect to HP 8131A Channel 1 Output	Connect to HP 8131A Channel 2 Output	Connect to HP 8131A Channel 2 Output
1	Pod 1, channel 3 Pod 3, channel 3 Pod 5, channel 3	Pod 2, channel 3 Pod 4, channel 3 Pod 6, channel 3	J-clock L-clock N-clock	K-clock M-clock P-clock
2	Pod 1, channel 11 Pod 3, channel 11 Pod 5, channel 11	Pod 2, channel 11 Pod 4, channel 11 Pod 6, channel 11	J-clock L-clock N-clock	K-clock M-clock P-clock



3 Activate the data channels that are connected according to the table on the previous page.

a Touch Listing, then select Format.

b Touch the field showing the channel assignments for one of the pods being tested. In the pop-up menu, touch clear. Using the knob, move the cursor to the data channels to be tested. Touch the asterisk field to put asterisks in the channel positions, activating the channels, then touch Done. Follow this step for the remaining five pods.



Check the clock period

Using the oscilloscope, verify that the clock period is 20 ns.

1 Enable the pulse generator channel 1 and channel 2 outputs (with the LED off).

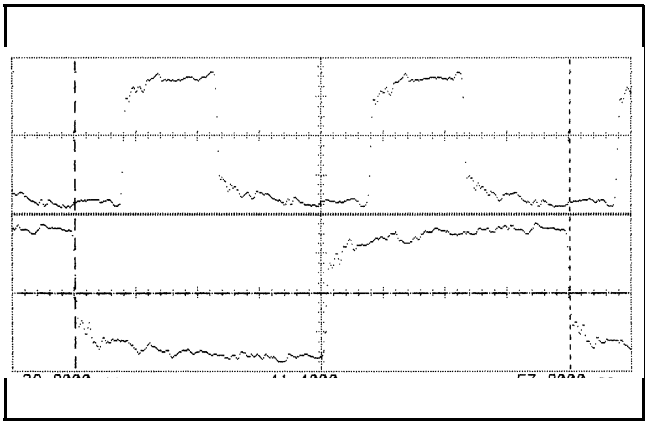
2 In the oscilloscope Timebase menu, select Sweep Speed 2.50 ns/div.

3 Select Delay. Using the oscilloscope knob, position the clock waveform so that a falling edge appears at the left of the display.

4 In the oscilloscope Measure menu, select Measure Chan 2, then select Period. If the period is less than 20.000 ns, go to the next page. If the period is not less than 20.000 ns, go to step 5.

5 In the oscilloscope Timebase menu, add 10 ns to the Delay.

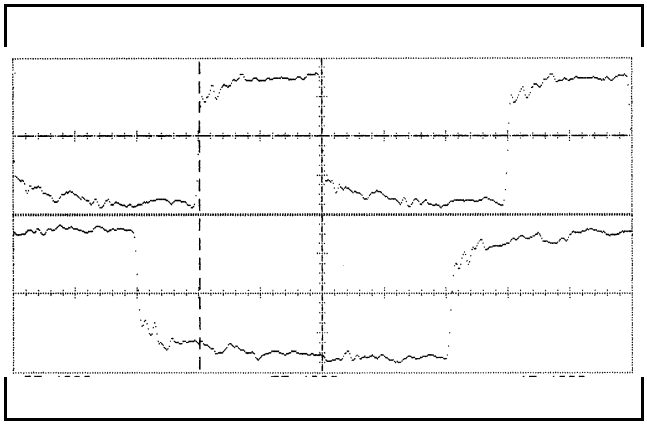
6 In the oscilloscope Measure menu, select Period. If the period is not less than 20.000 ns, decrease the pulse generator period in 100 ps increments until one of the two periods measured is less than 20.000 ns.



Check the data pulse width

Using the oscilloscope, verify that the data pulse width is 3.950 ns, +50 ps or –100 ps..

1. In the oscilloscope Timebase menu, select Sweep Speed 2.00 ns/div.
2. Select Delay. Using the oscilloscope knob, position the data waveform so that the falling edge of the waveform is centered on the screen.
3. In the oscilloscope Delta V menu, select Marker 1 Position Chan 1, Marker 1 at –1.3000 V. Select Marker 2 Position Chan 1, Marker 2 at –1.3000 V.
4. In the oscilloscope Delta t menu, select Start On Pos Edge 1. Select Stop on Neg Edge 1.
5. If the pulse width is outside of the limits, adjust the pulse generator channel 1 width



and select the oscilloscope Precision Edge Find until the pulse width is within limits.

Check the setup/hold with single clock, multiple clock edges

1 Select the logic analyzer setup/hold time.

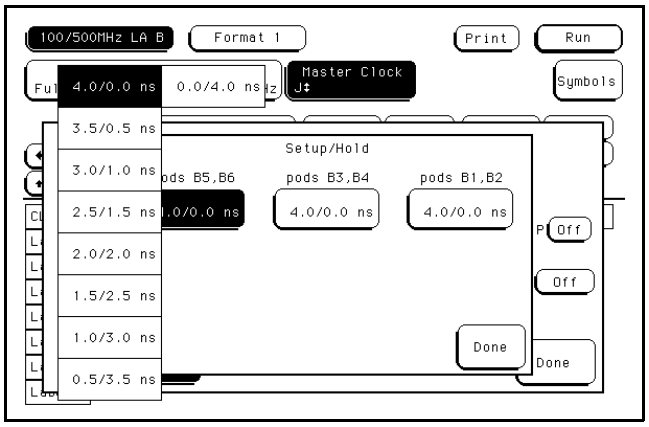
a In the logic analyzer Format menu, touch Master Clock.

b Select and activate any multiple clock edge.

c Touch the Setup/Hold field and select the setup/hold to be tested for all pods. The first time through this test, select the top combination in the following table.

Setup/Hold Combinations
4.0/0.0 ns
0.0/4.0 ns
2.0/2.0 ns

d Touch Done to exit the setup/hold combinations.



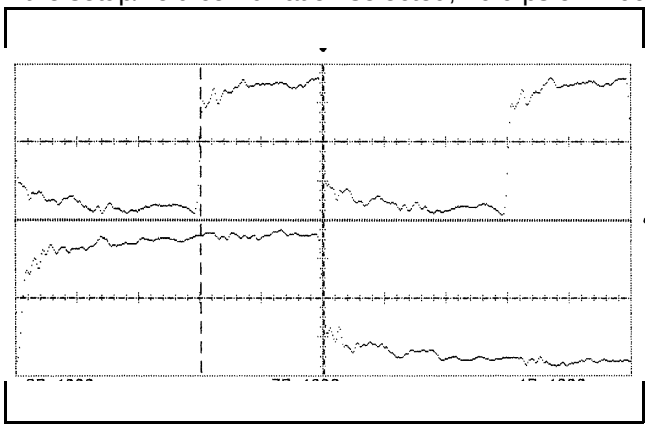
2 Disable the pulse generator channel 1 COMP (with the LED off).

3 Using the Delay mode of the pulse generator channel 2, position the pulses according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps.

a In the oscilloscope Delta V menu, select Marker 1 Position Chan 1, Marker 1 at –1.3000 V. Select Marker 2 Position Chan 2, Marker 2 at –1.3000 V.

b In the oscilloscope Delta t menu, select Start on Pos Edge 1. Select Stop on Neg Edge 1.

c Adjust the pulse generator channel 1 Delay and select Precision Edge Find in the oscilloscope Delta t menu until the pulses are aligned according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps.

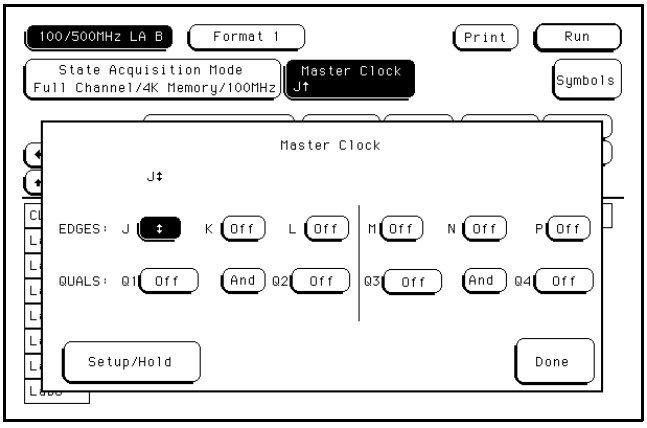


4 Select the clock to be tested.

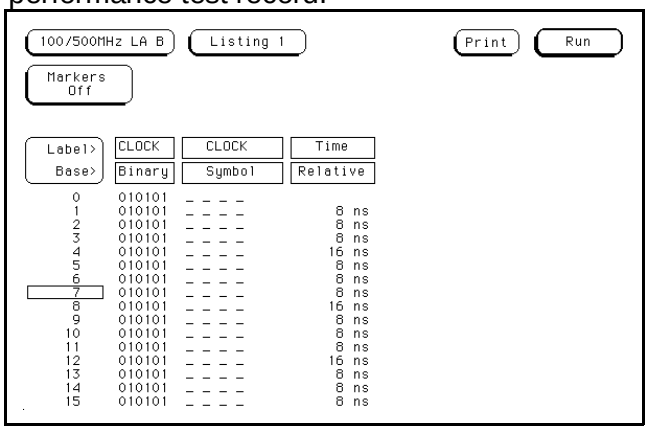
a Touch the clock field to be tested and then select the clock as indicated in the table. The first time through this test, select the top multiple-edge clock.

Clocks
J↕
K↕
L↕
M↕
N↕
P↕

b Touch Done to exit the Master Clock menu.



5 In the logic analyzer Format menu, touch Run. The display should show the pattern 010101 and the symbols column should show all "_ _ _ _." Verify the pattern by scrolling through the display. Record the Pass or Fail results in the performance test record.



6 Test the next clock.

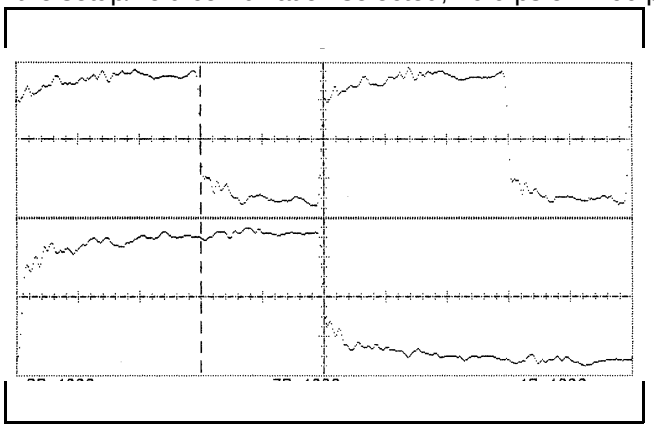
- **a** In the logic analyzer Format menu, touch Master Clock.
- **b** Turn off the clock just tested.
- **c** Repeat steps 4, 5, and 6 for the next clock listed in the table in step 4, until all listed clocks have been tested.

7 Enable the pulse generator channel 1 COMP (with the LED on).

8 Using the Delay mode of the pulse generator channel 2, position the pulses according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps.

- **a** In the oscilloscope Delta V menu, select Marker 1 Position Chan 1, Marker 1 at –1.3000 V. Select Marker 2 Position Chan 2, Marker 2 at –1.3000 V.
- **b** In the oscilloscope Delta t menu, select Start on Neg Edge 1. Select Stop on Neg Edge 1.

c Adjust the pulse generator channel 1 Delay and select Precision Edge Find in the oscilloscope Delta t menu until the pulses are aligned according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps.

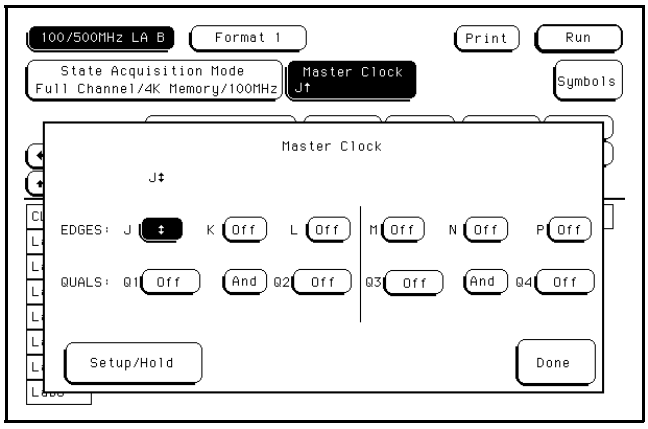


9 Select the clock to be tested.

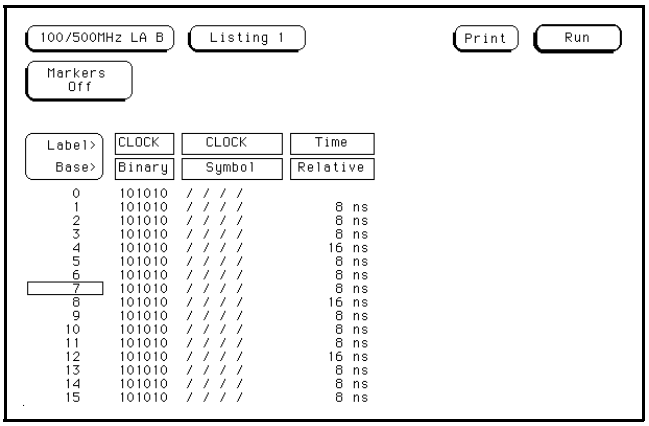
a Touch the clock field to be tested and then select the clock as indicated in the table. The first time through this test, select the top multiple-edge clock.

Clocks
J↕
K↕
L↕
M↕
N↕
P↕

b Touch Done to exit the Master Clock menu.



10 In the logic analyzer Format menu, touch Run. The display should show the pattern 101010 and the symbols column should show all "/ / / /." Verify the pattern by scrolling through the display. Record the Pass or Fail results in the performance test record.



11 Test the next clock.

- **a** In the logic analyzer Format menu, touch Master Clock.
- **b** Turn off the clock just tested.
- **c** Repeat steps 9, 10, and 11 for the next clock listed in the table in step 9, until all listed clocks have been tested.

12 Test the next setup/hold combination.

- **a** In the logic analyzer Format menu, touch Master Clock.
- **b** Turn off the clock just tested.
- **c** Repeat steps 1 through 12 for the next setup/hold combination listed in step 1 on page 3–55, until all listed setup/hold combinations have been tested.

When aligning the data and clock waveforms using the oscilloscope, align the waveforms according to the setup time of the setup/hold combination being tested, +0.0 ps or –100 ps.

Test the next channels

- Connect the next combination of data channels and clock channels, then test them.

  Start on page 3–52, "Connect the logic analyzer," connect the next combination, then continue through the complete test.

To test the time interval accuracy

Testing the time interval accuracy does not check a specification, but does check the following:

- 125 MHz oscillator

Two-card modules must be reconfigured as one-card modules for this test.

This test verifies that the 125 MHz timing acquisition synchronizing oscillator is operating within limits.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	100 MHz 3.5 ns pulse width, <600 ps rise time	HP 8131A Option 020
Function Generator	Accuracy $\leq (5)(10^{-6}) \times$ frequency	HP 3325B Option 002
SMA Cable		HP 8120-4948
Adapter	BNC(m)-SMA(f)	HP 1250-2015
BNC Test Connector, 6x2		

Set up the equipment

1. Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes if you have not already done so.
2. Set up the pulse generator according to the following table.

Pulse Generator Setup

Channel 1	Period	Mode	EXT TRIG
Delay: 0 ps	5 ns	TRIG	Slope: Positive
Width: 2.5 us			THRE: 1.0 V
High: –0.9 V			
Low: –1.7 V			
COMP: Disabled (LED off)			

3 Set up the function generator according to the following table.

Function Generator Setup	
Freq: 200 000 . 0 Hz	Main Function: Square wave
Amptd: 3.000 V	High Voltage: Disabled (LED Off)
Phase: 0.0 deg	
DC Offset: 0.0 V	

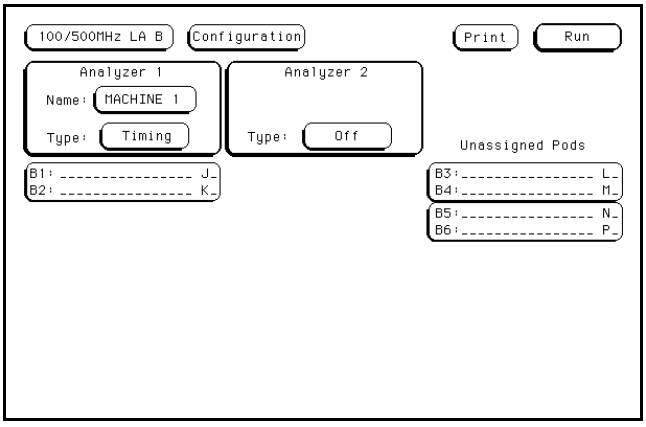
Set up the logic analyzer

1 Set up the Configuration menu.

a In the System Configuration menu, touch System, then select 100/500 MHz LA.

b In the Configuration menu, assign Pod 1 to Machine 1. To assign Pod 1, touch the Pod 1 field, then select Machine 1.

c In the Analyzer 1 box, touch the Type field, then select Timing.



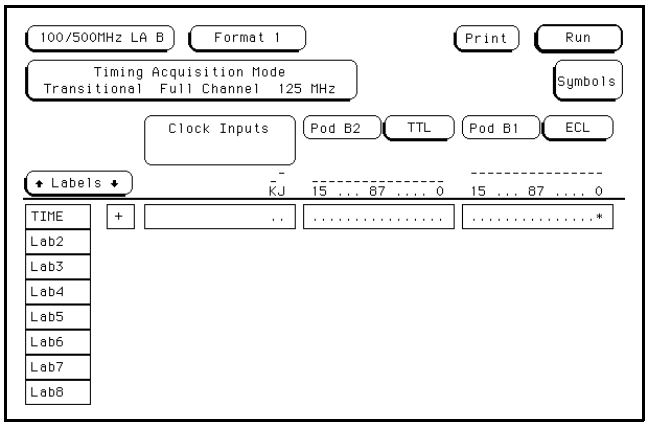
2 Set up the Format menu.

a Touch Configuration, then select Format. In the Format menu, touch Timing Acquisition Mode, then select Transitional Full Channel 125 MHz.

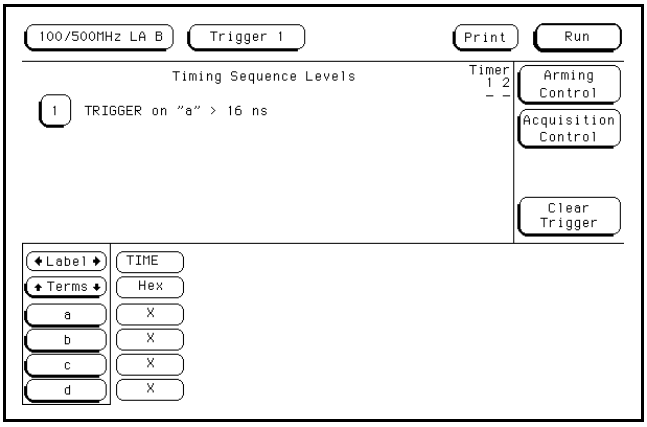
b Touch the field to the right of the Pod 1 field, then select ECL.

c Touch the field showing the channel assignments for Pod 1. Deactivate all channels by selecting Clear. Using the knob, move the cursor to Channel 0. Touch the asterisk field to put an asterisk in the channel position, activating the channel, then touch Done.

d Touch the top label, then select Modify Label. In the pop-up, type Time then touch Done.



3 Touch Format, then select Trigger. In the Trigger menu, touch Clear Trigger, then select All.



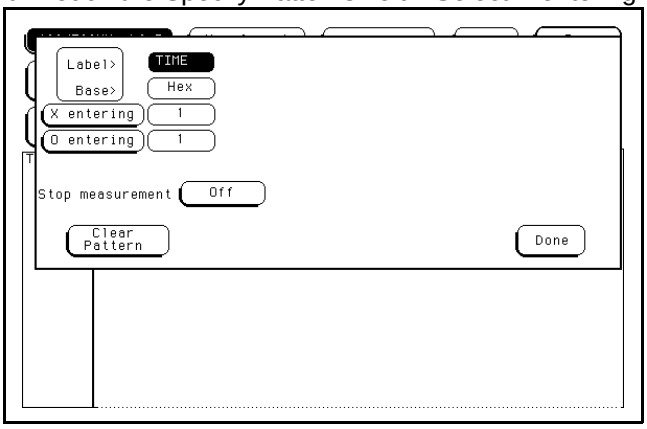
4 Set up the Waveform menu.

a Touch Trigger, then select Waveform.

b Touch the sec/Div field. In the pop-up menu, type 20 µs, then touch Done.

c Touch the Markers Off field, then select Pattern.

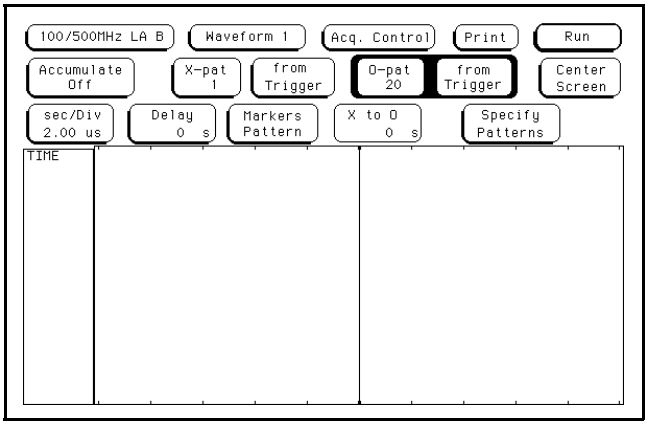
d Touch the Specify Patterns field. Select X entering 1 and O entering 1.



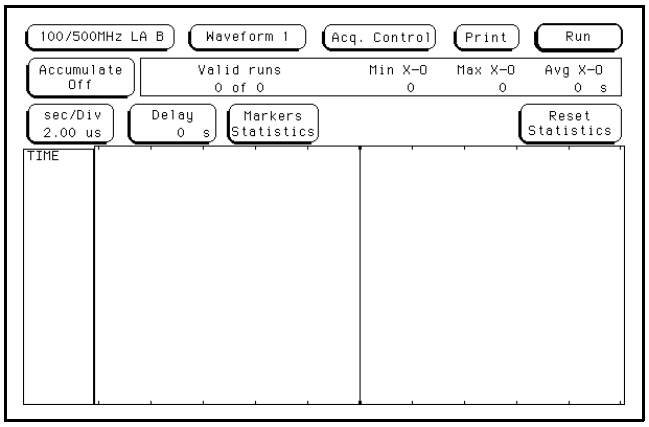
e Touch Done to exit the Specify Patterns menu.

f Touch the X-pat field twice. In the pop-up menu, select "1" and touch Done.

g Touch the O-pat field twice. In the pop-up menu, select "20" and touch Done.



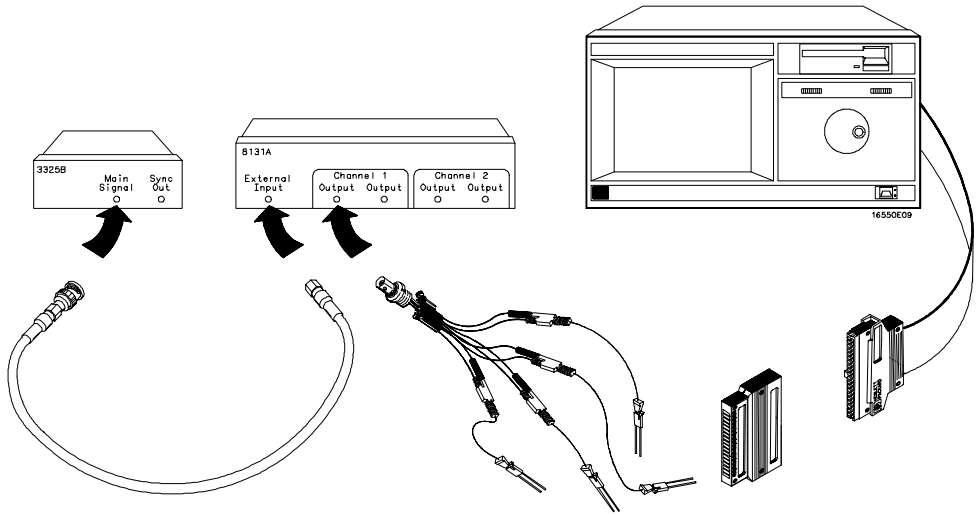
h Touch the Markers Patterns field and select Statistics. Touch Reset Statistics to initialize the statistics fields.



Connect the logic analyzer

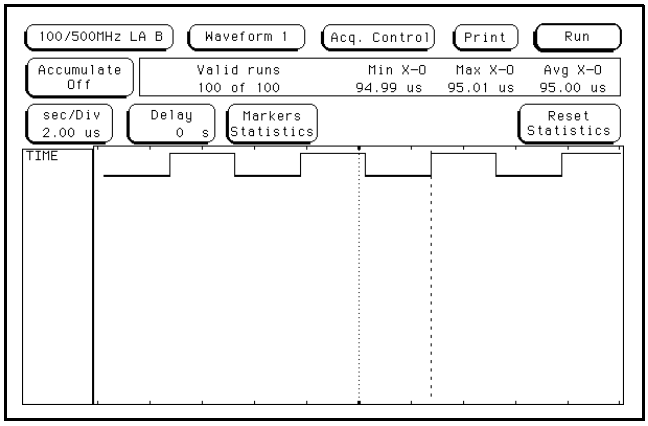
1 Using a 6-by-2 test connector, connect channel 0 of Pod 1 to the pulse generator channel 1 output.

2 Using the SMA cable and the BNC adapter, connect the External Input of the pulse generator to the Main Signal of the function generator.



Acquire the data

1. Enable the pulse generator channel 1 output (with the LED off).
2. In the logic analyzer Waveform menu, touch Run-Repetitive. Allow the logic analyzer to acquire data for at least 100 valid runs as indicated in the pattern statistics field.
3. When the logic analyzer has acquired more than 100 valid runs, touch Stop. The Min X-O field in the logic analyzer Pattern Statistics menu should read 94.99–95.00 µs. The Max X-O field should read 95.00–95.01 µs. The Avg X-O



field should read 95.00 µs. Record the results in the performance test record.

To perform the two-card test

Performing the two-card test verifies the performance of the following specifications:

- Minimum master to master clock time.
- Maximum state acquisition speed.

Two-card modules that were changed to one-card modules for the previous performance tests need to be reconfigured as a two-card module for this test.

This test checks a two-card module using one combination of data channels and a single-edge clock at one setup/hold time.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	100 MHz 3.5 ns pulse width, <600 ps rise time	HP 8131A option 020
Digitizing Oscilloscope	≥ 6 GHz bandwidth, <58 ps rise time	HP 54121T
Adapter	SMA(m)-BNC(f)	HP 1250-1200
SMA Coax Cable (Qty 3)		HP 8120-4948
Coupler	BNC(m-m)	HP 1250-0216
BNC Test Connector, 6x2 (Qty 4)		

Set up the equipment

1 Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes before beginning the test if you have not already done so.

2 Set up the pulse generator.

a Set up the pulse generator according to the following table.

Pulse Generator Setup

Channel 1	Channel 2	Period
Delay: 0 ps	Doub: 10.0 ns	20 ns
Width: 3.5 ns	Width: 3.5 ns	
High: –0.9 V	High: –0.9 V	
Low: –1.7 V	Low: –1.7 V	

b Enable the pulse generator channel 2 COMP (with the LED on).

3 Set up the oscilloscope.

Oscilloscope Setup

Time Base	**Display**	**Delta V**	**Delta t**
Time/Div: 1.00 ns/div	avg	V markers on	T markers on
	# of avg: 16	marker 1 position: Chan 1	start on: Pos Edge 1
	screen: dual	marker 2 position: Chan 1	stop on: Neg Edge 1

Channel

	Channel 1	**Channel 2**
Display	on	on
Probe Atten	20.00	20.00
Offset	–1.3 V	–1.3 V
Volts/Div	400 mV	400 mV

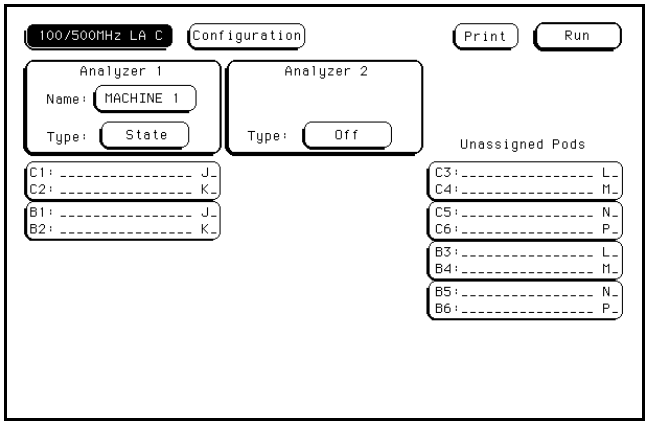
Set up the logic analyzer

1 Set up the Configuration menu.

a In the System Configuration menu, touch System, then select 100/500 MHz LA.

b In the Configuration menu, assign pods 1 and 2 of the master and the expander card to Machine 1. To assign the pods, touch the pod fields, then select Machine 1.

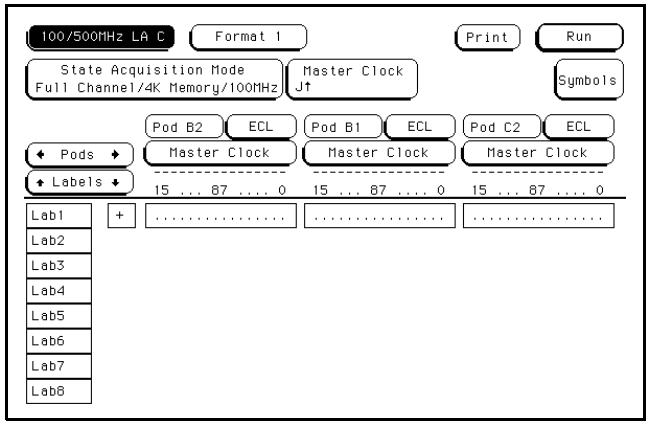
c In the Analyzer 1 box, touch the Type field, then select State.



2 Set up the Format menu.

a Touch Configuration, then select Format. In the Format menu, touch State Acquisition Mode, then select Full Channel/4K Memory/100MHz.

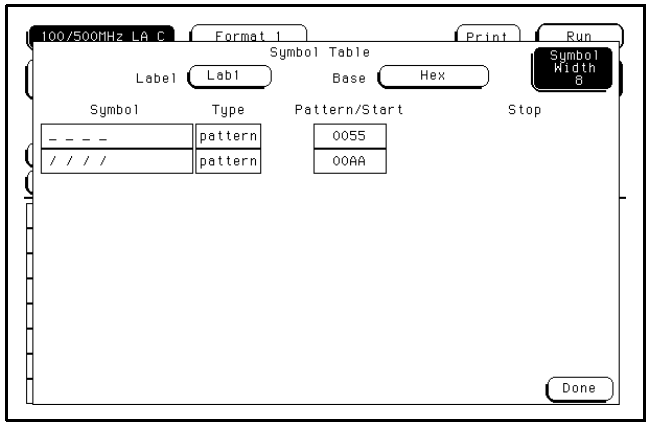
b Touch the field to the right of each Pod field, then select ECL. The screen does not show all Pod fields at one time. To access more Pod fields, turn the knob.



3 Set up the Symbols menu.

a Touch Symbols, then touch New symbol. In the pop-up menu, type "_ _ _ _," then touch Done. Touch the Pattern/Start field. In the pop-up menu, type "0055," then touch done.

b Touch the Symbol field, then select Add a Symbol. In the pop-up menu, type "////," then touch Done. Touch the Pattern/Start field on the same line as the "////" symbols. In the pop-up menu, type "00AA," then touch Done. Touch Done to exit Symbols.



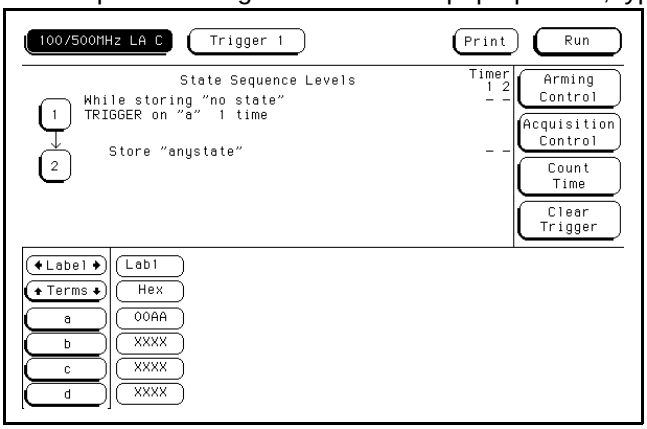
4 Set up the Trigger menu.

a Touch Configuration, then select Trigger. In the Trigger menu, touch Clear Trigger, then select All.

b Touch Count, touch off, then select Time. Touch Done to exit the Count menu.

c Touch the field labeled 1 under the State Sequence Levels. Touch the field labeled "anystate," then select "no state." Touch done.

d Touch pattern recognizer "a." In the pop-up menu, type "00AA," then touch Done.

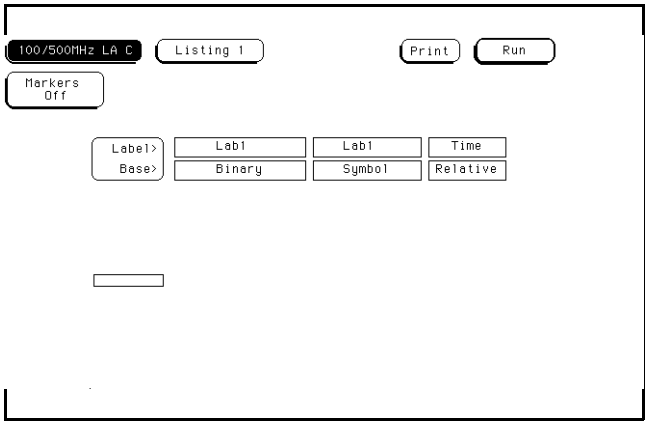


5 Set up the Listing menu.

a Touch the Lab1 base field, then select Binary.

b Touch the Lab1 label field, select Insert, then select Lab1.

c Touch the Base field below the second Lab1 label, then select Symbol.



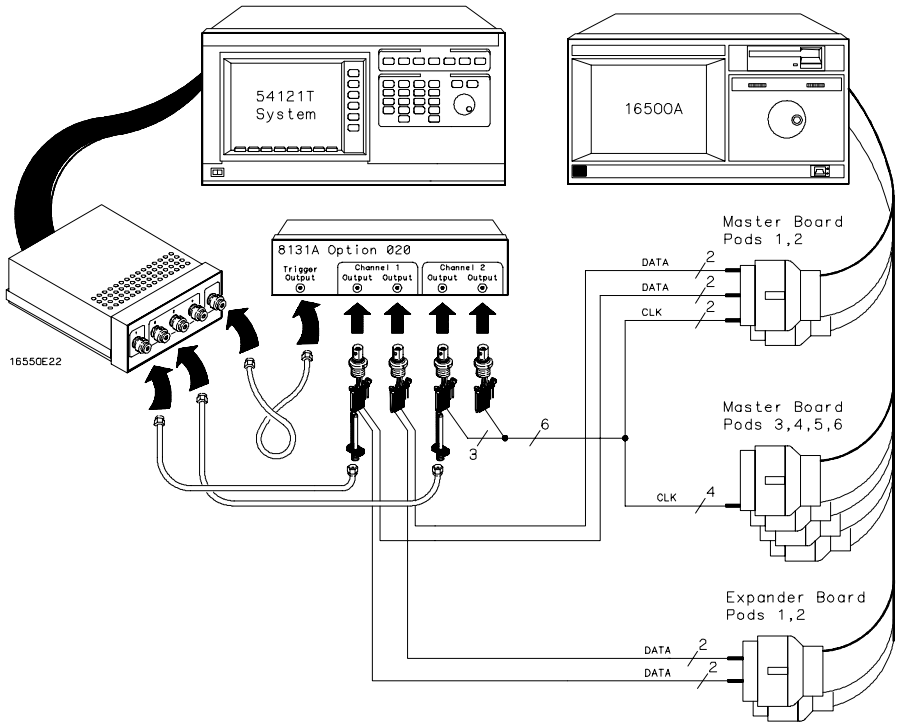
Connect the logic analyzer

1 Using the 6-by-2 test connectors, connect the first combination of logic analyzer clock and data channels listed the table below to the pulse generator.

2 Using SMA cables, connect channel 1, channel 2, and trigger from the oscilloscope to the pulse generator.

Connect the Logic Analyzer to the Pulse Generator

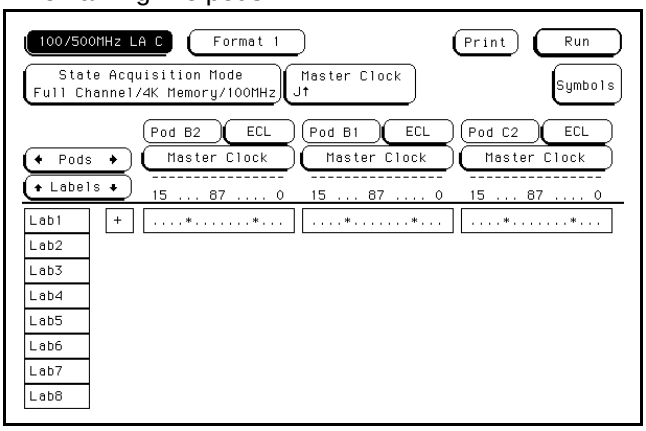
	Connect to HP 8131A Channel 1 Output	Connect to HP 8131A Channel 1 Output	Connect to HP 8131A Channel 2 Output	Connect to HP 8131A Channel 2 Output
Master Board	Pod 1, channel 3 Pod 2, channel 3	Pod 1, channel 11 Pod 2, channel 11	J-clock L-clock N-clock	K-clock M-clock P-clock
Expander Board	Pod 1, channel 3 Pod 2, channel 3	Pod 1, channel 11 Pod 2, channel 11		



3 Activate the data channels that are connected according to the table on the previous page.

a Touch Listing, then select Format.

b Touch the field showing the channel assignments for one of the pods being tested. In the pop-up menu, touch clear. Using the knob, move the cursor to the data channels to be tested. Touch the asterisk field to put asterisks in the channel positions, activating the channels, then touch Done. Follow this step for the remaining five pods.



Check the clock pulse width

Using the oscilloscope, verify that the clock pulse width is 3.45 ns, +50 ps or -100 ps.

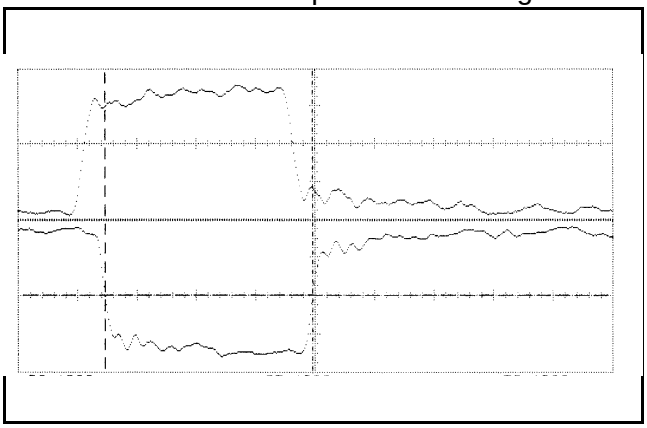
1 Enable the pulse generator channel 1 and channel 2 outputs.

2 In the oscilloscope Timebase menu, select Delay. Using the oscilloscope knob, position the clock waveform so that the waveform is centered on the screen.

3 In the oscilloscope Delta V menu, select Marker 1 Position Chan 2, Marker 1 at –1.3000 V. Select Marker 2 Position Chan 2, Marker 2 at –1.3000 V.

4 In the oscilloscope Delta t menu, select Start On Neg Edge 1. Select Stop on Pos Edge 1.

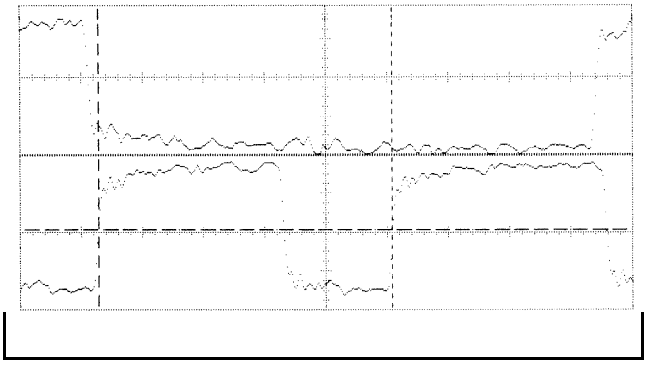
5 If the pulse width is outside the limits, adjust the pulse generator channel 2 width and select the oscilloscope Precision Edge Find until the pulse width is within limits.



Check the clock period

Using the oscilloscope, verify that the clock period is 10 ns.

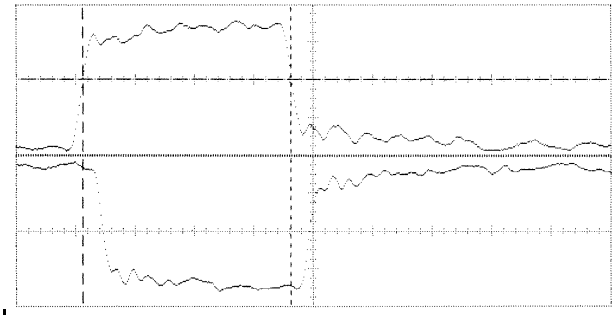
1. In the oscilloscope Timebase menu, select Sweep Speed 2.00 ns/div.
2. Select Delay. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.
3. In the oscilloscope Measure menu, select Measure Chan 2, then select Period. If the period is not less then 10.000 ns, go to step 4. If the period is less then 10.000 ns, go to the next page.
4. In the oscilloscope Timebase menu, add 10 ns to the delay.
5. In the oscilloscope Measure menu, select Period. If the period is not less then 10.000 ns, decrease the pulse generator Chan 2 Doub in 10 ps increments until one of the two periods measured is less then 10.000 ns.



Check the data pulse width

Using the oscilloscope, verify that the data pulse width is 3.45 ns +50 ps or -100 ps.

1. In the oscilloscope Timebase menu, select Sweep Speed 1.00 ns/div.
2. Select Delay. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.
3. In the oscilloscope Delta V menu, select Marker 1 Position Chan 1, Marker 1 at –1.300 V. Select Marker 2 position Chan 1, marker 2 at –1.3000 V.
4. In the oscilloscope Delta t menu, select Start On Pos Edge 1. Select Stop on Neg Edge 1.
5. Select Precision Edge Find.
6. If the pulse width is outside the limits, adjust the pulse generator channel 1 width



and select the oscilloscope Precision Edge Find until the pulse width is within limits.

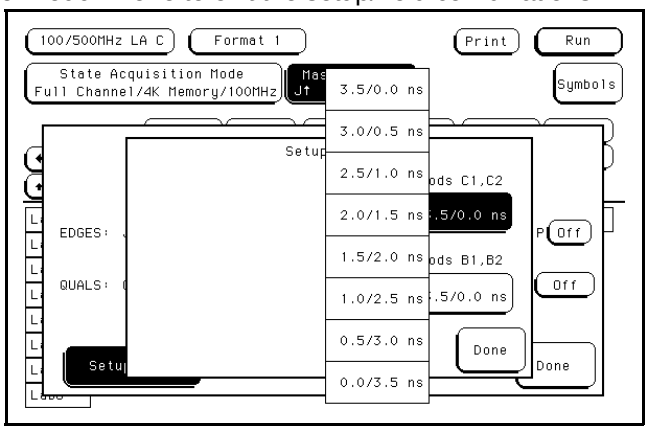
Check the setup/hold combination

1 Select the logic analyzer setup/hold time.

a In the logic analyzer Format menu, touch Master Clock.

b Touch the Setup/Hold field and select the 3.5/0.0 ns setup/hold combination to be tested for all pods.

c Touch Done to exit the setup/hold combinations.



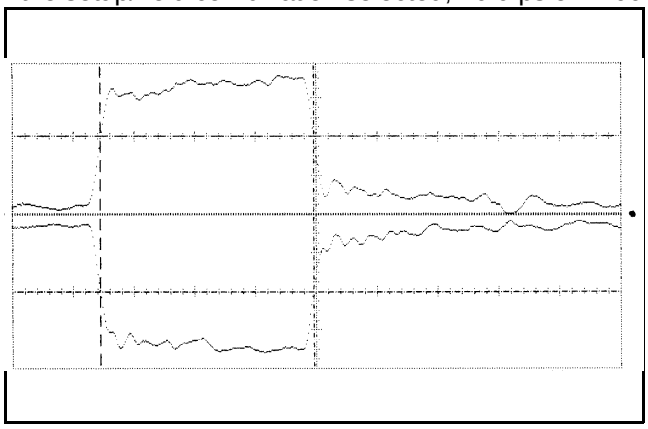
2 Enable the pulse generator channel 2 COMP (with the LED on).

3 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or –100 ps.

a In the oscilloscope Delta V menu, select Marker 1 Position Chan 1, Marker 1 at –1.3000 V. Select Marker 2 Position Chan 2, Marker 2 at –1.3000 V.

b In the oscilloscope Delta t menu, select Start on Pos Edge 1. Select Stop on Pos Edge 1.

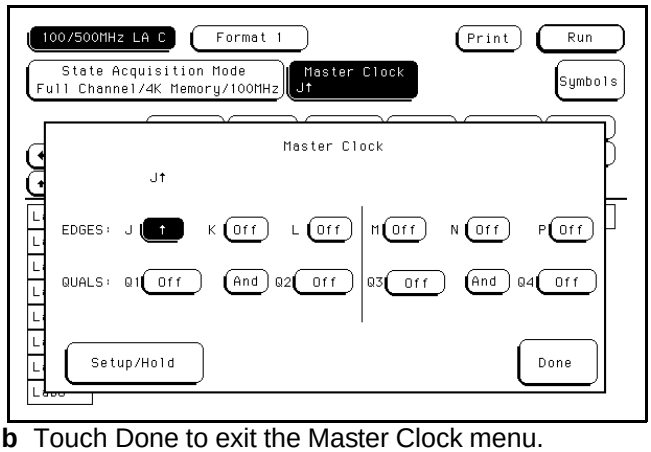
c Adjust the pulse generator channel 1 Delay and select Precision Edge Find in the oscilloscope Delta t menu until the pulses are aligned according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps.



4 Select the clock to be tested.

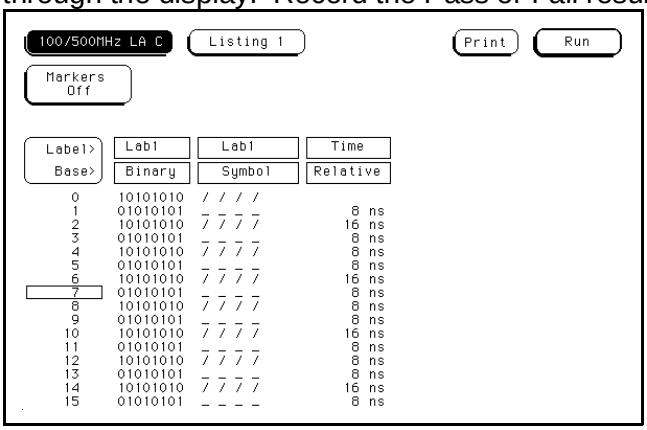
a Touch the clock field to be tested and then select the clock edge as indicated in the table. The first time through this test, select the top clock and edge.

Clocks
J↑
K↓
L↑
M↓
N↑
P↓



b Touch Done to exit the Master Clock menu.

5 In the logic analyzer Format menu, touch Run. The display should show a checkerboard pattern of alternating 1s and 0s, and the symbols column should show alternating lines of "_ _ _ _" and "/ / / /." Verify the pattern by scrolling through the display. Record the Pass or Fail results in the performance test record.



6 Test the next clock.

a In the logic analyzer Format menu, touch Master Clock.

b Turn off the clock just tested.

c Repeat steps 4, 5, and 6 for the next clock edge listed in the table in step 4, until all listed clock edges have been tested.

Performance Test Record

HEWLETT PACKARD

HP 16550A 100-MHz State, 500-MHz Timing Logic Analyzer_____

Serial No._____ Work Order No._____

Recommended Test Interval - 2 Year/4000 hours Date_____

Recommended next testing_____ Temperature_____

Test	Settings		Results	
Self-Tests			Pass/Fail	_____
Threshold Accuracy	± (100 mV + 3% of threshold setting)			
			Limits	Measured
Pod 1	TTL, ±145 mV	TTL VL	+1.355 V	_____
		TTL VH	+1.645 V	_____
	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	-User, ±280 mV	-User VL	-6.280 V	_____
		- User VH	-5.720 V	_____
	+User, ±280 mV	+ User VL	+5.720 V	_____
		+ User VH	+6.280 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____
Pod 2	TTL, ±145 mV	TTL VL	+1.355 V	_____
		TTL VH	+1.645 V	_____
	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	-User, ±280 mV	-User VL	-6.280 V	_____
		- User VH	-5.720 V	_____
	+User, ±280 mV	+ User VL	+5.720 V	_____
		+ User VH	+6.280 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____

Test	**Settings**		**Results**	
Pod 3	TTL, ±145 mV	TTL VL	+1.355 V	_____
		TTL VH	+1.645 V	_____
	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	-User, ±280 mV	-User VL	-6.280 V	_____
		- User VH	-5.720 V	_____
	+User, ±280 mV	+ User VL	+5.720 V	_____
		+ User VH	+6.280 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____

Performance Test Record (continued)

Test	Settings		Results	
Threshold Accuracy (continued)			Limits	Measured
Pod 4	TTL, ±145 mV	TTL VL	+1.355 V	_____
		TTL VH	+1.645 V	_____
	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	-User, ±280 mV	-User VL	-6.280 V	_____
		- User VH	-5.720 V	_____
	+User, ±280 mV	+ User VL	+5.720 V	_____
		+ User VH	+6.280 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____
Pod 5	TTL, ±145 mV	TTL VL	+1.355 V	_____
		TTL VH	+1.645 V	_____
	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	-User, ±280 mV	-User VL	-6.280 V	_____
		- User VH	-5.720 V	_____
	+User, ±280 mV	+ User VL	+5.720 V	_____
		+ User VH	+6.280 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____
Pod 6	TTL, ±145 mV	TTL VL	+1.355 V	_____
		TTL VH	+1.645 V	_____
	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	-User, ±280 mV	-User VL	-6.280 V	_____
		- User VH	-5.720 V	_____
	+User, ±280 mV	+ User VL	+5.720 V	_____
		+ User VH	+6.280 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____
Glitch Capture	Minimum Detectable Glitch 3.5 ns			Pass/Fail
		Pod 1		_____
		Pod 2		_____
		Pod 3		_____
		Pod 4		_____
		Pod 5		_____
		Pod 6		_____

Test	Settings	Results

Performance Test Record (continued)

Test	Settings		Results			
Single-Clock, Single-Edge Acquisition				Pass/Fail		Pass/Fail
All Pods, Channel 3	Setup/Hold Time	3.5/0.0 ns	J↑ K↓ L↑ M↓ N↑ P↓	_____ _____ _____ _____ _____	J↓ K↑ L↓ M↑ N↓ P↑	_____ _____ _____ _____ _____
	Setup/Hold Time	0.0/3.5 ns	J↑ K↓ L↑ M↓ N↑ P↓	_____ _____ _____ _____ _____	J↓ K↑ L↓ M↑ N↓ P↑	_____ _____ _____ _____ _____
	Setup/Hold Time	1.5/2.5 ns	J↑ K↓ L↑ M↓ N↑ P↓	_____ _____ _____ _____ _____	J↓ K↑ L↓ M↑ N↓ P↑	_____ _____ _____ _____ _____
All Pods, Channel 11	Setup/Hold Time	3.5/0.0 ns	J↑ K↓ L↑ M↓ N↑ P↓	_____ _____ _____ _____ _____	J↓ K↑ L↓ M↑ N↓ P↑	_____ _____ _____ _____ _____
	Setup/Hold Time	0.0/3.5 ns	J↑ K↓ L↑ M↓ N↑ P↓	_____ _____ _____ _____ _____	J↓ K↑ L↓ M↑ N↓ P↑	_____ _____ _____ _____ _____

Test	Settings		Results			
	Setup/Hold Time	1.5/2.5 ns	J↑	_____	J↓	_____
			K↓	_____	K↑	_____
			L↑	_____	L↓	_____
			M↓	_____	M↑	_____
			N↑	_____	N↓	_____
			P↓		P↑	

Performance Test Record (continued)

Test	Settings		Results			
Multiple-Clock, Multiple-Edge Acquisition			Enable pulse generator, channel 2 COMP (LED on)		Disable pulse generator, channel 2 COMP (LED off)	
				Pass/Fail		Pass/Fail
All Pods, Channel 3	Setup/Hold Time	4.5/0.0 ns	J↑ + M↓ + N↑	_____	J↓ + M↑ + N↓	_____
			K↓ + L↑ + P↓	_____	K↑ + L↓ + P↑	_____
	Setup/Hold Time	0.0/4.5 ns	J↑ + M↓ + N↑	_____	J↓ + M↑ + N↓	_____
			K↓ + L↑ + P↓	_____	K↑ + L↓ + P↑	_____
	Setup/Hold Time	2.0/2.5 ns	J↑ + M↓ + N↑	_____	J↓ + M↑ + N↓	_____
			K↓ + L↑ + P↓	_____	K↑ + L↓ + P↑	_____
All Pods, Channel 11	Setup/Hold Time	4.5/0.0 ns	J↑ + M↓ + N↑	_____	J↓ + M↑ + N↓	_____
			K↓ + L↑ + P↓	_____	K↑ + L↓ + P↑	_____
	Setup/Hold Time	0.0/4.5 ns	J↑ + M↓ + N↑	_____	J↓ + M↑ + N↓	_____
			K↓ + L↑ + P↓	_____	K↑ + L↓ + P↑	_____
	Setup/Hold Time	2.0/2.5 ns	J↑ + M↓ + N↑	_____	J↓ + M↑ + N↓	_____
			K↓ + L↑ + P↓	_____	K↑ + L↓ + P↑	_____

Test	Settings	Results

Performance Test Record (continued)

Test	Settings		Results			
Single-Clock, Multiple-Edge Acquisition			Disable pulse generator, channel 1 COMP (LED off)		Enable pulse generator, channel 1 COMP (LED on)	
				Pass/Fail		Pass/Fail
All Pods, Channel 3	Setup/Hold Time	4.0/0.0 ns	J↕ K↕ L↕ M↕ N↕ P↕	_____ _____ _____ _____ _____ _____	J↕ K↕ L↕ M↕ N↕ P↕	_____ _____ _____ _____ _____ _____
	Setup/Hold Time	0.0/4.0 ns	J↕ K↕ L↕ M↕ N↕ P↕	_____ _____ _____ _____ _____ _____	J↕ K↕ L↕ M↕ N↕ P↕	_____ _____ _____ _____ _____ _____
	Setup/Hold Time	2.0/2.0 ns	J↕ K↕ L↕ M↕ N↕ P↕	_____ _____ _____ _____ _____	J↕ K↕ L↕ M↕ N↕ P↕	_____ _____ _____ _____ _____
All Pods, Channel 11	Setup/Hold Time	4.0/0.0 ns	J↕ K↕ L↕ M↕ N↕ P↕	_____ _____ _____ _____ _____	J↕ K↕ L↕ M↕ N↕ P↕	_____ _____ _____ _____ _____
	Setup/Hold Time	0.0/4.0 ns	J↕ K↕ L↕ M↕ N↕ P↕	_____ _____ _____ _____ _____ _____	J↕ K↕ L↕ M↕ N↕ P↕	_____ _____ _____ _____ _____ _____
	Setup/Hold Time	2.0/2.0 ns	J↕ K↕ L↕ M↕ N↕ P↕	_____ _____ _____ _____ _____ _____	J↕ K↕ L↕ M↕ N↕ P↕	_____ _____ _____ _____ _____ _____

Test	Settings	Results

Performance Test Record (continued)

Test	Settings		Results	
Time Interval Accuracy				Measured
	min X-0	94.99-95.00 µs		_____
	max X-0	95.00-95.01 µs		_____
	avg X-0	94.99-95.01 µs		_____
Two-Card Test				
	Setup/Hold Time	3.5/0.0 ns		Pass/Fail
			J↑	_____
			K↓	_____
			L↑	_____
			M↓	_____
			N↑	_____
			P↓	

4

Calibrating

Calibrating

This chapter gives you instructions for calibrating the logic analyzer.

Calibration Strategy

The HP 16550A logic analyzer requires no calibrating. To periodically verify the performance of the analyzer, refer to "Testing Performance" in chapter 3.

5

Troubleshooting

Troubleshooting

This chapter helps you troubleshoot the module to find defective assemblies. The troubleshooting consists of flowcharts, self-test instructions, a cable test, and a test for the auxiliary power supplied by the probe cable. This information is not intended for component-level repair.

If you suspect a problem, start at the top of the first flowchart. During the troubleshooting instructions, the flowcharts will direct you to perform the self-tests or the cable test.

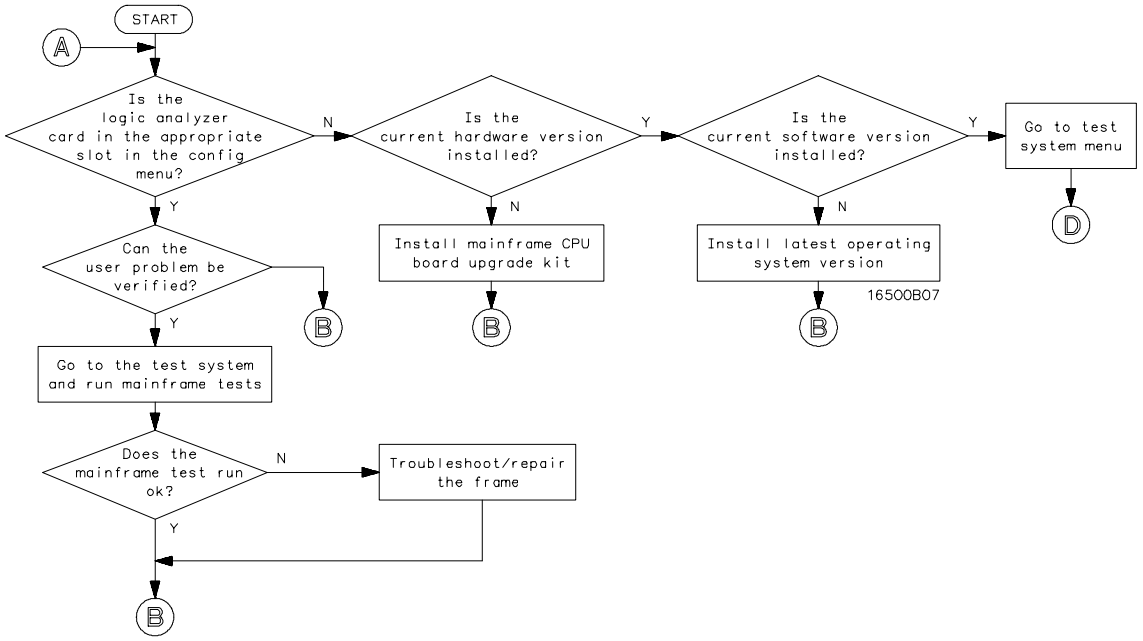
The service strategy for this instrument is the replacement of defective assemblies. This module can be returned to Hewlett-Packard for all service work, including troubleshooting. Contact your nearest Hewlett-Packard Sales Office for more details.

CAUTION

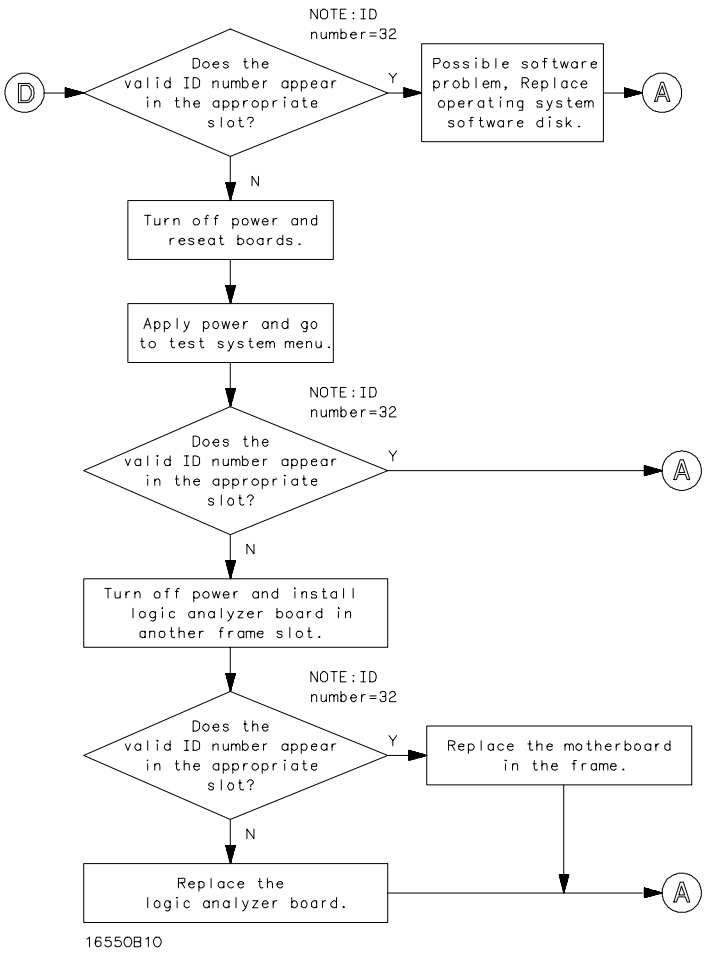
Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when you perform any service to this instrument or to the cards in it.

To use the flowcharts

Flowcharts are the primary tool used to isolate defective assemblies. The flowcharts refer to other tests to help isolate the trouble. The circled letters on the charts indicate connections with the other flowcharts. Start your troubleshooting at the top of the first flowchart.



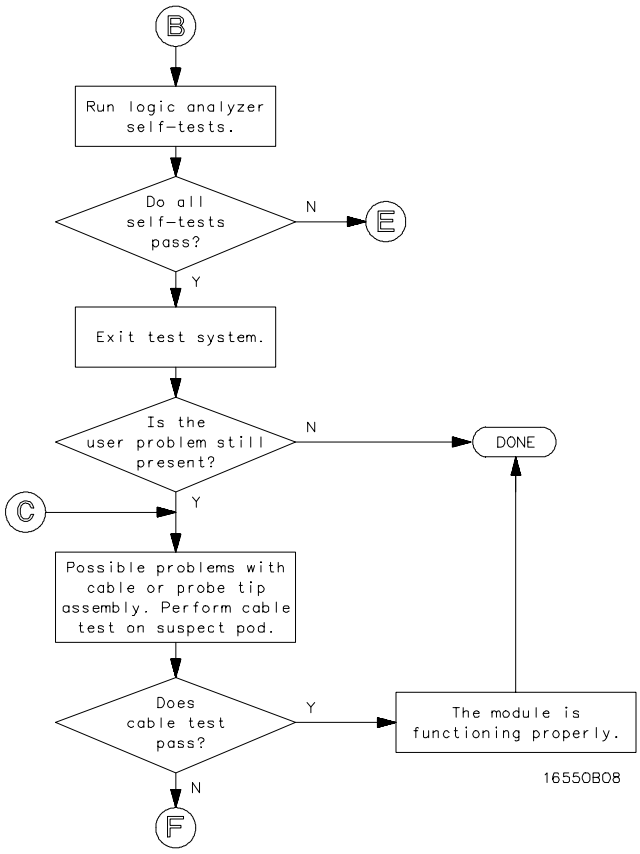
Troubleshooting Flowchart 1



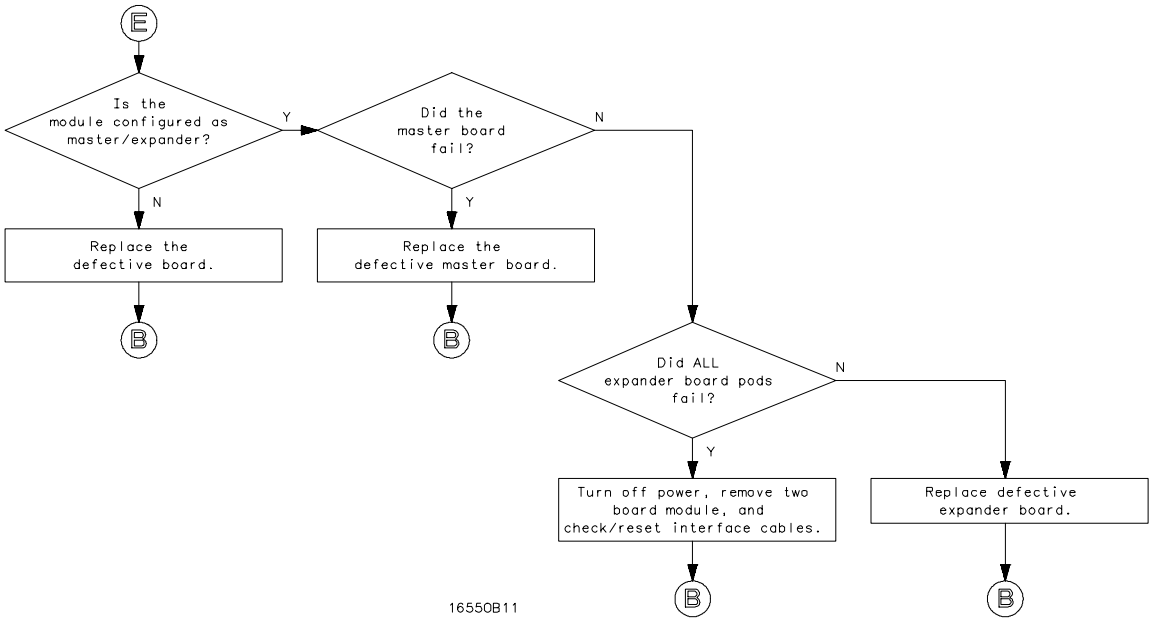
Troubleshooting Flowchart 2

See "To run the self-tests," page 5-8.

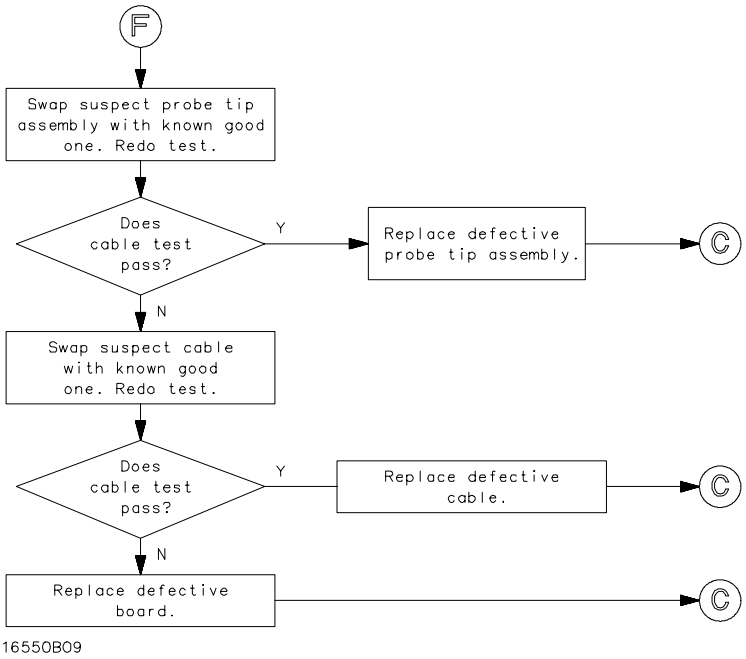
See "To test the cables," page 5-12.



Troubleshooting Flowchart 3



Troubleshooting Flowchart 4

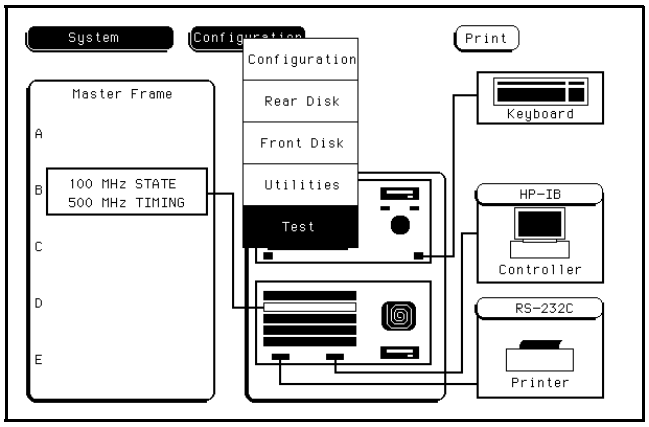


Troubleshooting Flowchart 5

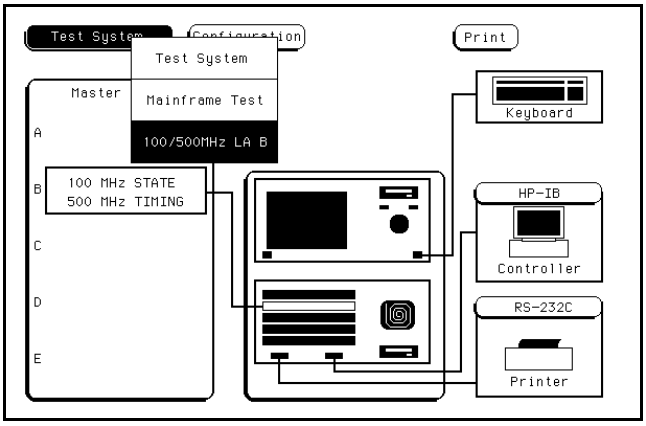
To run the self-tests

Self-tests for the module identify the correct operation of major functional areas of the module. You can run all self-tests without accessing the interior of the instrument. If a self-test fails, the troubleshooting flowcharts instruct you to change a card or cable of the module.

1. Disconnect all inputs, insert the disk containing the operating system into a disk drive, then turn on the power switch.
2. In the System Configuration menu, touch Configuration. In the pop-up menu, touch Test.

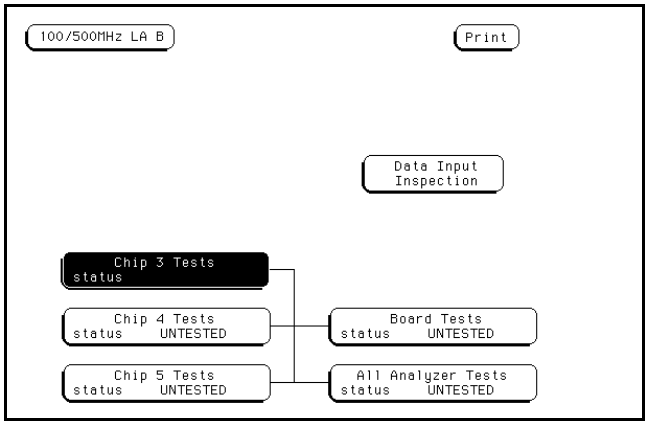


3. Remove the operating system disk, then insert the disk containing the performance verification tests (self-tests) into the disk drive. Touch the box labeled Touch box to Load Test System.
4. In the test system screen, touch Test System. Select the 100 MHz/500 MHz LA module to be tested.



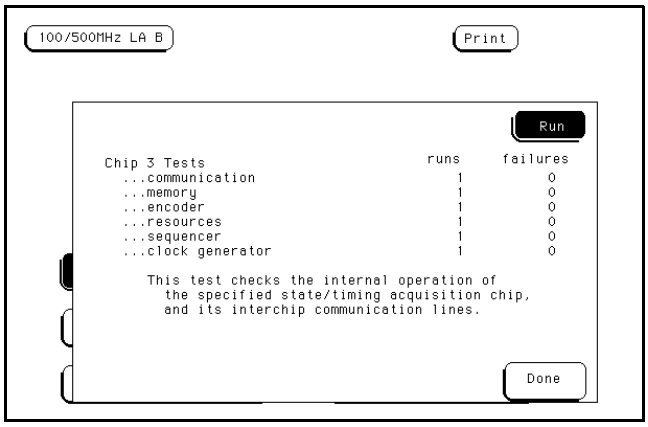
5 Touch Chip 3 Tests.

You can run all tests at one time by touching All Analyzer Tests. To see more details about each test, you can run each test individually. This example shows how to run Chip 3 Tests. Chip 4 and 5 Tests operate the same as Chip 3 Tests.



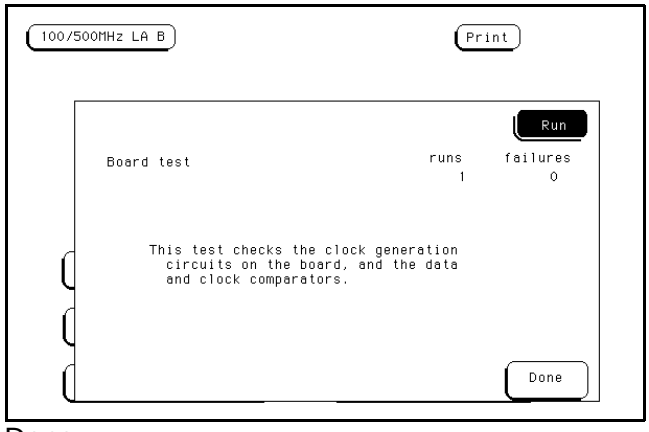
6 In the Chip 3 Tests menu, touch Run. The test runs one time, and the screen shows the results.

To run a test continuously, touch and hold your finger on Run. Drag your finger to Repetitive, then lift your finger. Touch Stop to stop Run Repetitive.



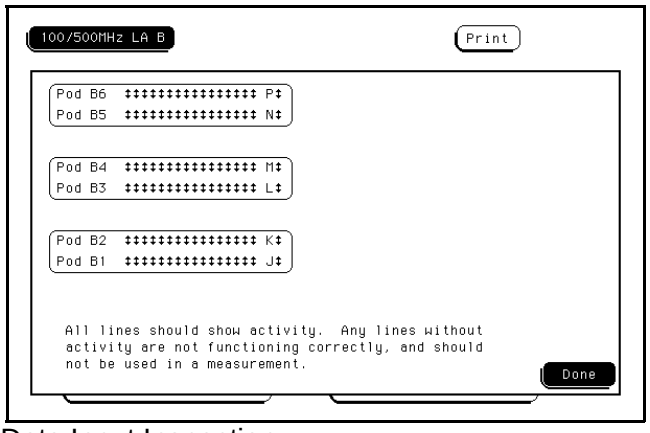
7 When the test is finished, touch Done. Then, perform Chip 4 and 5 Tests.

8 Touch Board Tests, then touch Run. When the Board Tests are finished, touch



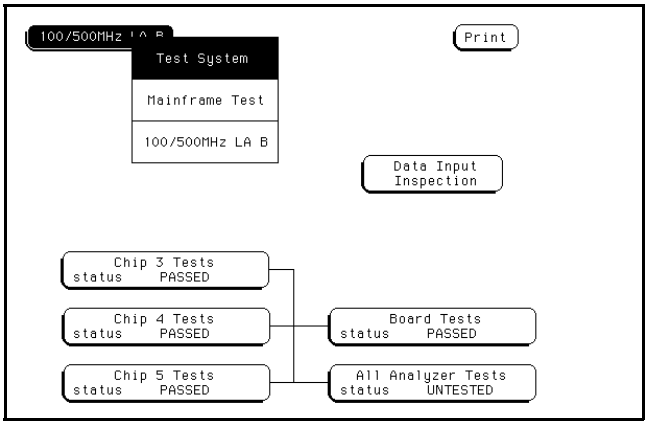
Done.

9 Touch Data Input Inspection. All lines should show activity. Touch Done to exit the



Data Input Inspection.

10 To exit the test screen, touch 100/500 MHz LA, then select Test System.



11 To exit the test system, touch Configuration, then select Exit Test. Remove the performance verification disk, then insert the operating system disk into a disk drive. Touch the box labeled Touch box to Exit Test System.

12 If you are performing the self-tests as part of the troubleshooting flowchart, return to troubleshooting flowchart 3, page 5-5.

To test the cables

This test allows you to functionally verify the probe cable and probe tip assembly of any of the logic analyzer pods. Only one probe cable can be tested at a time. Repeat this test for each probe cable to be tested.

Equipment Required

Equipment	Critical Specification	Recommended Model/Part
Pulse Generator	100 MHz, 3.5 ns pulse width, < 600 ps rise time	HP 8131A Option 020
6x2 Test Connectors (Qty 4)		

1 Turn on the equipment required and the logic analyzer.

2 Set up the pulse generator.

a Set up the pulse generator according to the following table.

Pulse Generator Setup

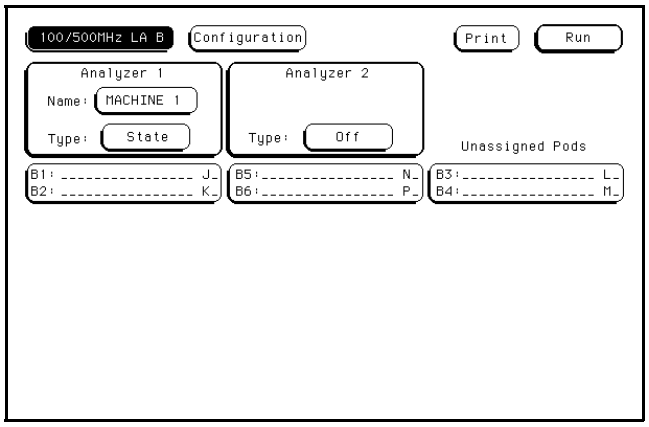
Channel 1	Channel 2	Period
Delay: 0 ps	Delay: 0 ps	100 ns
Dty: 50%	Dty: 50%	
High: 3.00 V	High: 3.00 V	
Low: 0.00 V	Low: 0.00 V	

b Enable the pulse generator channel 1 and channel 2 outputs (with the LEDs off).

3 Set up the logic analyzer Configuration menu.

a In the System Configuration menu, touch System, then select 100/500 MHz LA.

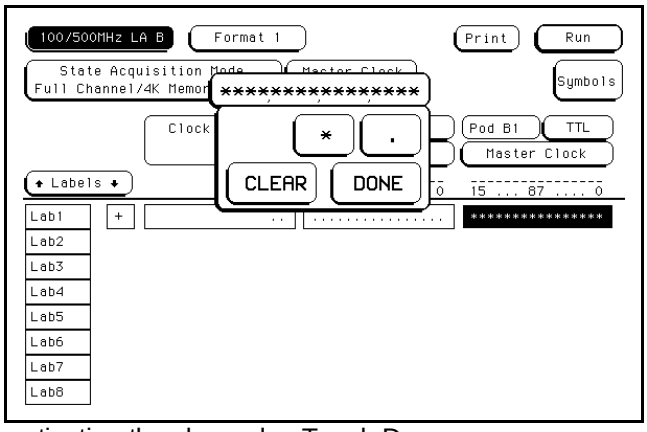
b In the Analyzer 1 box, touch the field to the right of Type, then select State.



4 Set up the Format menu.

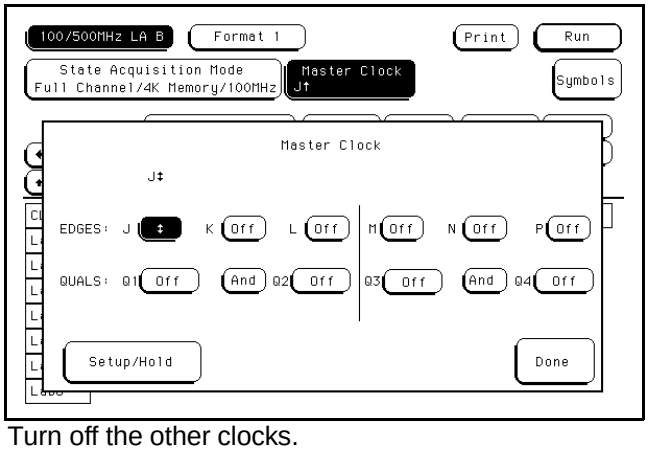
a Touch Configuration, then select Format.

b Touch the field showing the channel assignments for the pod under test. In the pop-up menu, touch the asterisk field to put asterisks in the channel positions,



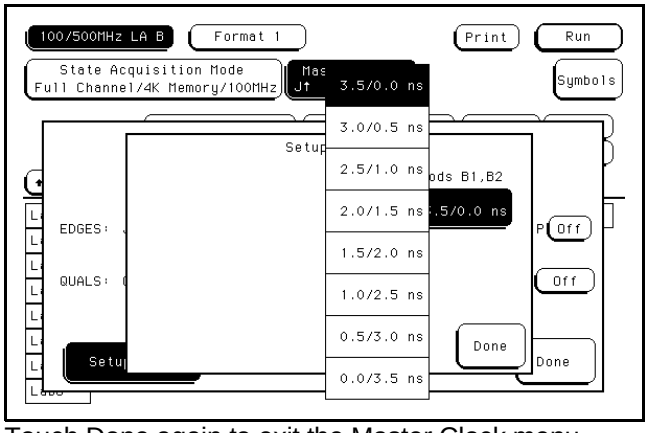
activating the channels. Touch Done.

c Touch Master Clock, then select a double edge for the clock of the pod under test.

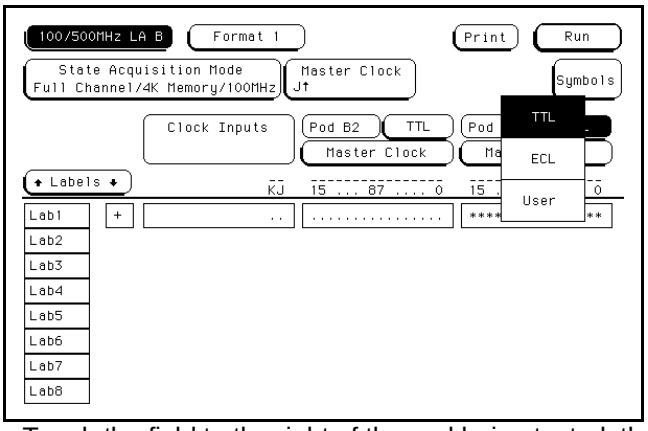


Turn off the other clocks.

d Touch Setup/Hold, then select 3.5 ns/0.0 ns for the pod being tested. Touch Done.



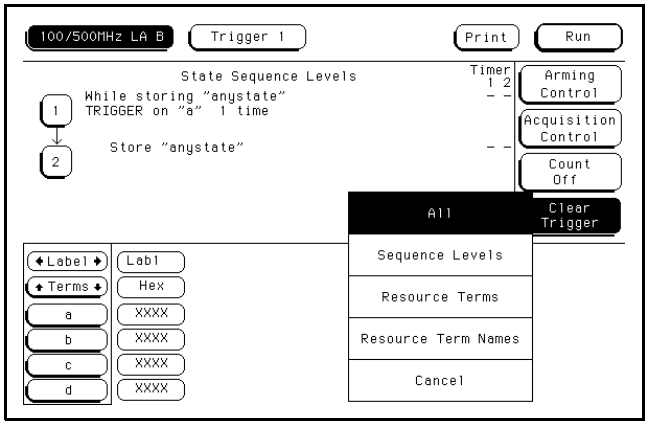
Touch Done again to exit the Master Clock menu.



e Touch the field to the right of the pod being tested, then select TTL.

5 Set up the Trigger menu.

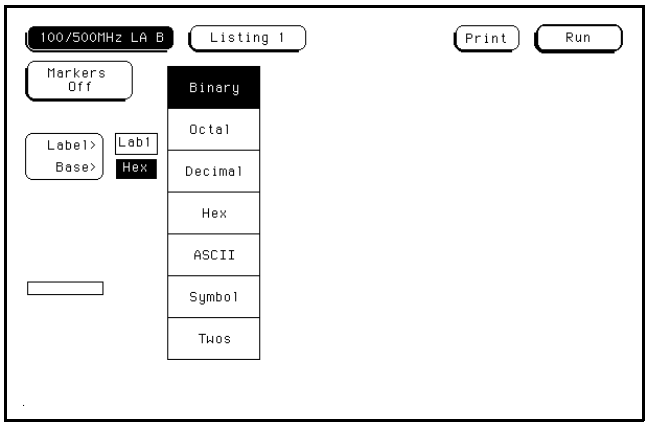
a Touch Format, then select Trigger.



b Touch Clear Trigger, then select All.

6 Set up the Listing menu.

a Touch Trigger, then select Listing.



b Touch the field to the right of Base, then select Binary.

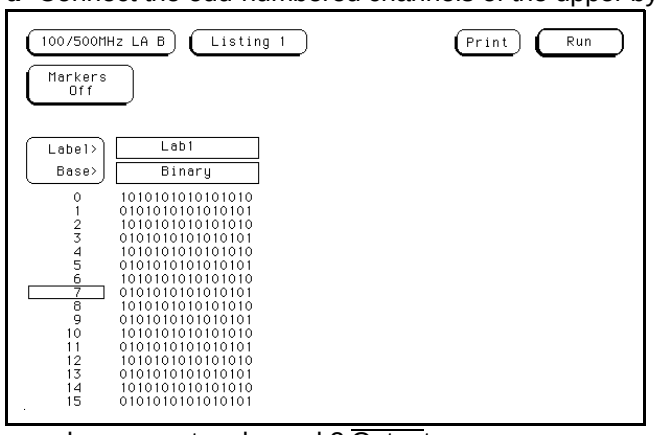
7 Using four 6-by-2 test connectors, connect the logic analyzer to the pulse generator channel outputs. To make the test connectors, ‘see chapter 3, "Testing Performance."

a Connect the even-numbered channels of the lower byte of the pod under test to the pulse generator channel 1 Output.

b Connect the odd-numbered channels of the lower byte of the pod under test to the pulse generator channel 1 $\overline{\text{Output}}$.

c Connect the even-numbered channels of the upper byte of the pod under test and the clock channel to the pulse generator channel 2 Output.

d Connect the odd-numbered channels of the upper byte of the pod under test to the



pulse generator channel 2 $\overline{\text{Output}}$.

8 On the logic analyzer, touch Run. The display should look similar to the figure below.

9 If the display looks like the figure, then the cable passed the test.

If the display does not look similar to the figure, then there is a possible problem with the cable or probe tip assembly. Causes for cable test failures include:

- open channel.
- channel shorted to a neighboring channel.
- channel shorted to either ground or a supply voltage.

Return to the troubleshooting flowchart.

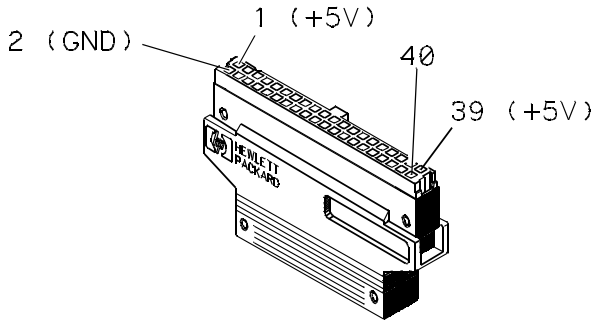
To test the auxiliary power

The +5 V auxiliary power is protected by a current overload protection circuit. If the current on pins 1 and 39 exceed 0.33 amps, the circuit will open. When the short is removed, the circuit will reset in approximately 1 minute. There should be +5 V after the 1 minute reset time.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Digital Multimeter	0.1 mV resolution, better than 0.005% accuracy	HP 3478A

- Using the multimeter, verify the +5 V on pins 1 and 39 of the probe cables.



MISC/EX50

6

Replacing Assemblies

Replacing Assemblies

This chapter contains the instructions for removing and replacing the logic analyzer module, the circuit board of the module, and the probe cables of the module. Also in this chapter are instructions for returning assemblies.

CAUTION Turn off the instrument before installing, removing, or replacing a module in the instrument.

Tools Required

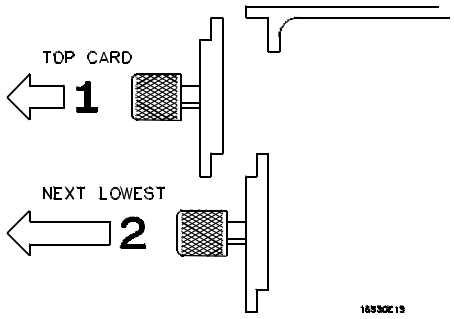
A T10 TORX screwdriver is required to remove screws connecting the probe cables and screws connecting the back panel.

To remove the module

CAUTION Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when performing any service to this module.

1. Turn off the instrument power switch, then unplug the power cord. Disconnect any input or output connections.
2. Loosen the thumb screws.

   Starting from the top, loosen the thumb screws on the filler panels and cards located above the module and the thumb screws of the module.



3. Starting from the top, pull the cards and filler panels located above the module half-way out.
4. If the module consists of a single card, pull the card completely out.

   If the module consists of two cards, pull both cards completely out.
5. Push all other cards into the card cage, but not completely in.

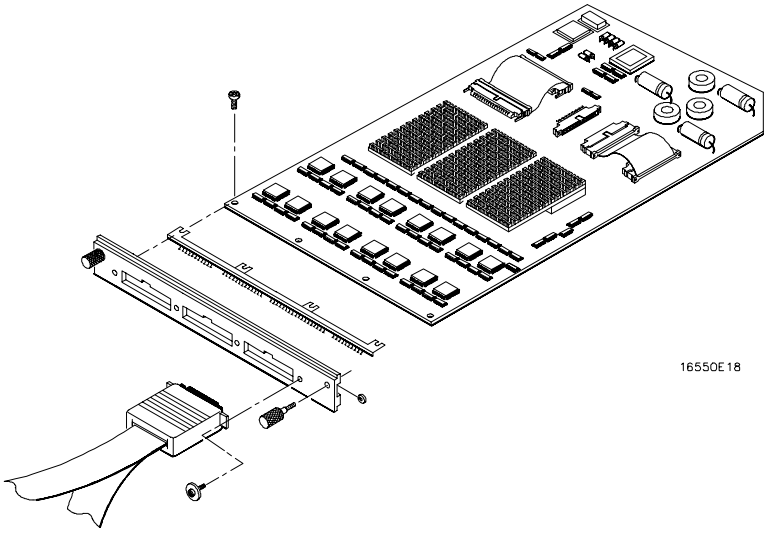
   This is to get them out of the way for removing and replacing the module.
6. If the module consist of a single card, remove the faulty card.

   If the module consists of two cards, remove the cables from J5 and J7 of the upper card. Remove the cable from J6 of the lower card. Replace the faulty card.

To replace the circuit board

1. Remove the four screws connecting the probe cables to the back panel, then disconnect the probe cables.
2. Remove the four screws attaching the ground spring and back panel to the circuit board, then remove the back panel and the ground spring.
3. Replace the faulty circuit board with a new circuit board. On the faulty board, make sure the 80-pin ribbon cable is connected between J4 and J5 and the 100-pin ribbon cable is connected between J7 and J8.
4. Position the ground spring and back panel on the back edge of the replacement circuit board. Install four screws to connect the back panel and ground spring to the circuit board.
5. Connect the probe cables, then install four screws to connect the cables to the back panel.

CAUTION If you over tighten the screws, the threaded inserts on the back panel might break off of the back panel. Tighten the screws only enough to hold the cable in place.



To replace the module

1 If the module consists of one card, go to step 2.

If the module consists of two cards, connect the cables as follows.

> Directions for connecting the cables are printed on the circuit board.

a Disconnect the two cables from J4 and J5 and from J7 and J8 on the card to go in the upper slot.

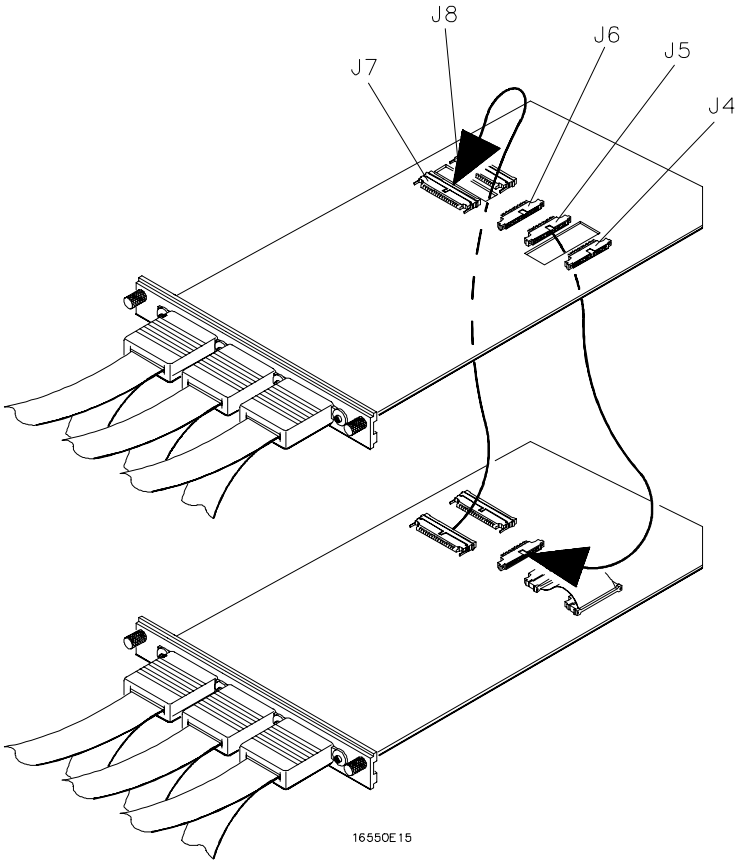
CAUTION

If you pull on the flexible ribbon part of the cable, you might damage the cable assembly. To remove a cable from the connector on the board, gently pry the hard plastic part of the ribbon cable away from the connector using a screwdriver.

b Disconnect the cable from J7 and J8 of the card to go in the lower slot.

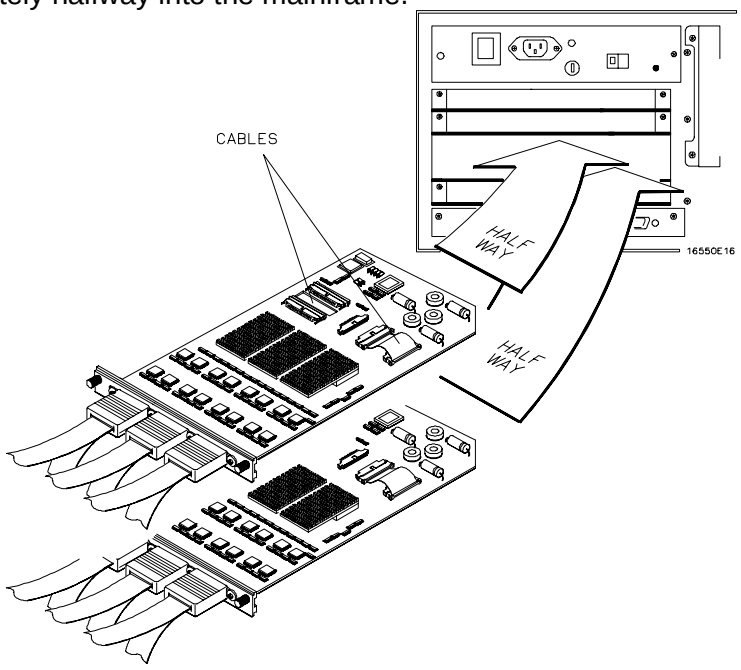
c Connect the 80-pin cable from J6 of the lower card to J5 of the upper card. The cable between J4 and J5 of the lower card should remain connected.

d Connect the 100-pin cable from J7 of the lower card to J7 of the upper card.



2 Slide the cards above the slots for the module about halfway out of the mainframe.

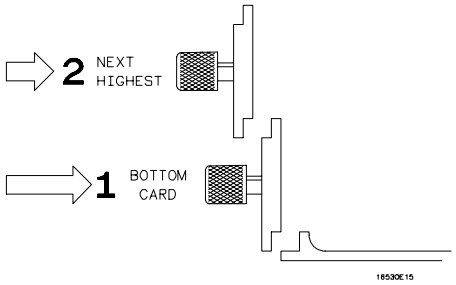
3 With the probe cables facing away from the instrument, slide the module approximately halfway into the mainframe.



4 Slide the complete module into the mainframe, but not completely in.

Each card in the instrument is firmly seated and tightened one at a time in step 6.

5 Position all cards and filler panels so that the endplates overlap.



6 Seat the cards and tighten the thumbscrews.

Starting with the bottom card, firmly seat the cards into the backplane connector of the mainframe. Keep applying pressure to the center of the card endplate while tightening the thumbscrews finger-tight. Repeat this for all cards and filler panels starting at the bottom and moving to the top.

CAUTION

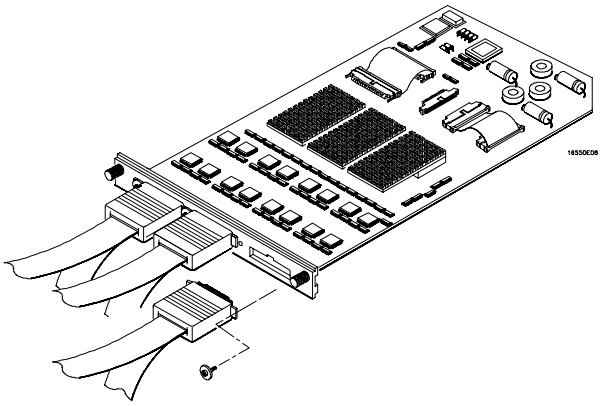
Correct air circulation keeps the instrument from overheating. For correct air circulation, filler panels must be installed in all unused card slots. Keep any extra filler panels for future use.

To replace the probe cable

1. Turn off the instrument power switch, then unplug the power cord. Disconnect any input or output connections.
2. Remove the screws that hold the probe cable to the rear panel of the module.
3. Remove the faulty probe cable from the connector and install the replacement cable.
4. Install the label on the new probe.

   If you order a new probe cable, you will need to order new labels. Probe cables shipped with the module are labeled. Probe cables shipped separately are not labeled. Refer to chapter 7, "Replaceable Parts," for the part numbers and ordering information.
5. Install the screws connecting the probe cable to the rear panel of the module.

CAUTION



If you over tighten the screws, the threaded inserts on the back panel might break off of the back panel. Tighten the screws only enough to hold the cable in place.

To return assemblies

Before shipping the module to Hewlett-Packard, contact your nearest Hewlett-Packard sales office for additional details.

1. Write the following information on a tag and attach it to the module.
   - Name and address of owner
   - Model number
   - Serial number
   - Description of service required or failure indications
2. Remove accessories from the module.

   Only return accessories to Hewlett-Packard if they are associated with the failure symptoms.
3. Package the module.

   You can use either the original shipping containers, or order materials from an HP sales office.

CAUTION

For protection against electrostatic discharge, package the module in electrostatic material.

4 Seal the shipping container securely, and mark it FRAGILE.

7

Replaceable Parts

Replaceable Parts

This chapter contains information for identifying and ordering replaceable parts for your module.

Replaceable Parts Ordering

Parts listed

To order a part on the list of replaceable parts, quote the Hewlett-Packard part number, indicate the quantity desired, and address the order to the nearest Hewlett-Packard Sales Office.

Parts not listed

To order a part not on the list of replaceable parts, include the model number and serial number of the module, a description of the part (including its function), and the number of parts required. Address the order to your nearest Hewlett-Packard Sales Office.

Direct mail order system

To order using the direct mail order system, contact your nearest Hewlett-Packard Sales Office.

Within the USA, Hewlett-Packard can supply parts through a direct mail order system. The advantages to the system are direct ordering and shipment from the HP Part Center in Mountain View, California. There is no maximum or minimum on any mail order. (There is a minimum amount for parts ordered through a local Hewlett-Packard Sales Office when the orders require billing and invoicing.) Transportation costs are prepaid (there is a small handling charge for each order) and no invoices.

In order for Hewlett-Packard to provide these advantages, a check or money order must accompany each order. Mail order forms and specific ordering information are available through your local Hewlett-Packard Sales Office. Addresses and telephone numbers are located in a separate document shipped with the *HP 16500A/16501A Logic Analysis System Service Manual.*

Exchange Assemblies

Some assemblies are part of an exchange program with Hewlett-Packard.

The exchange program allows you to exchange a faulty assembly with one that has been repaired and performance verified by Hewlett-Packard.

After you receive the exchange assembly, return the defective assembly to Hewlett-Packard. A United States customer has 30 days to return the defective assembly. If you do not return the defective assembly within the 30 days, Hewlett-Packard will charge you an additional amount. This amount is the difference in price between a new assembly and that of the exchange assembly. For orders not originating in the United States, contact your nearest Hewlett-Packard Sales Office for information.

See Also "To return assemblies," page 6–6.

Replaceable Parts List

The replaceable parts list is organized by reference designation and shows exchange assemblies, electrical assemblies, then other parts.

Information included for each part on the list consists of the following:

- Reference designator
- Hewlett-Packard part number
- Check Digit (CD)
- Total quantity included with the module (Qty)
- Description of the part

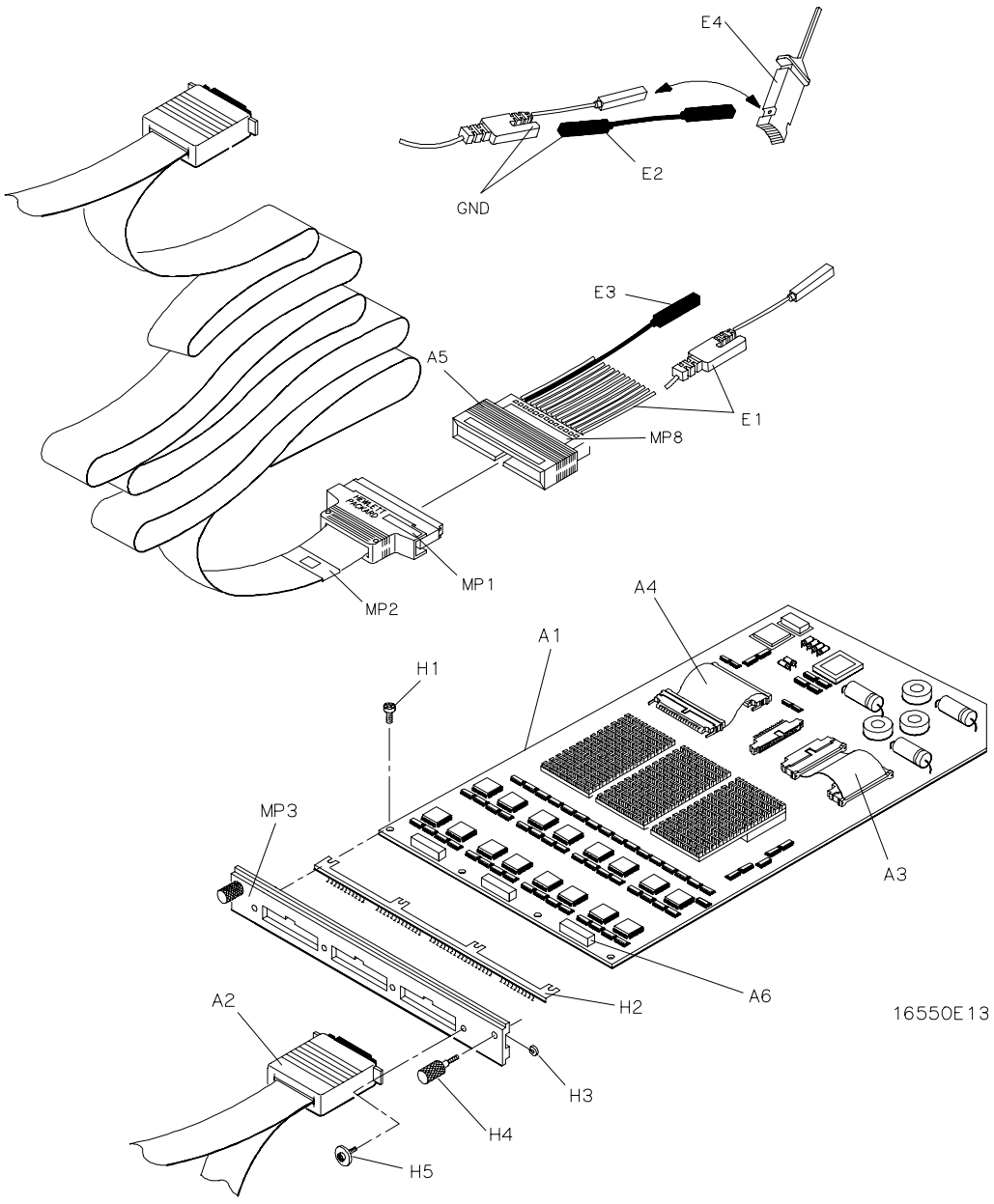
Reference designators used in the parts list are as follows:

- A Assembly
- H Hardware
- J Connector
- MP Mechanical Part
- W Cable

HP 16550A Replaceable Parts

Ref. Des.	HP Part Number	CD	QTY	Description
		Exchange Assemblies		
	16550-69501	4	1	Exchange Board Assembly
		HP 16550A		
A1	16550-66501	8	1	Board Assembly
A2	16550-61601	9	3	Cable Assembly-Logic Analyzer
A3	16550-61602	0	1	Cable Assembly-80 Pos IDC
A4	16550-61603	1	1	Cable Assembly-100 Pos IDC
A5	01650-61608	6	6	Probe Tip Assembly
A6	1252-4181	2	3	Probe Cable Socket - 50 pin
E1	5959-9333	8	1	Probe Leads Replace (5 Per Package)
E2	5959-9334	9	0	Probe Ground Replace (5 Per Package)
E3	5959-9335	0	0	Pod Ground Replace (2 Per Package)
E4	5090-4356	3	6	Grabber Kit Assembly (20 Grabbers Per Package)
H1	16500-22401	5	2	Panel Screw
H2	16650-29101	6	1	Ground Spring
H3	0510-0684	9	2	Retaining Ring
H4	0515-0430	3	4	MS M3.0X0.5X6MM PH T10 (Endplate Screw)
H5	0515-2306	6	4	Screw Sems M3 X 0.5X10mm (Cable Retaining Screw)
MP1	01650-94310	6	1	Label-Probe and Cable
MP2	16500-41201	3	1	Ribbon Cable ID Clip
MP3	16550-40501	4	1	Module Panel
MP4	16550-94301	5	1	Label-ID
MP5	7121-4650	9	1	Label-Antistatic

Exploded View



Exploded view of the HP 16550A logic analyzer.

8

Theory of Operation

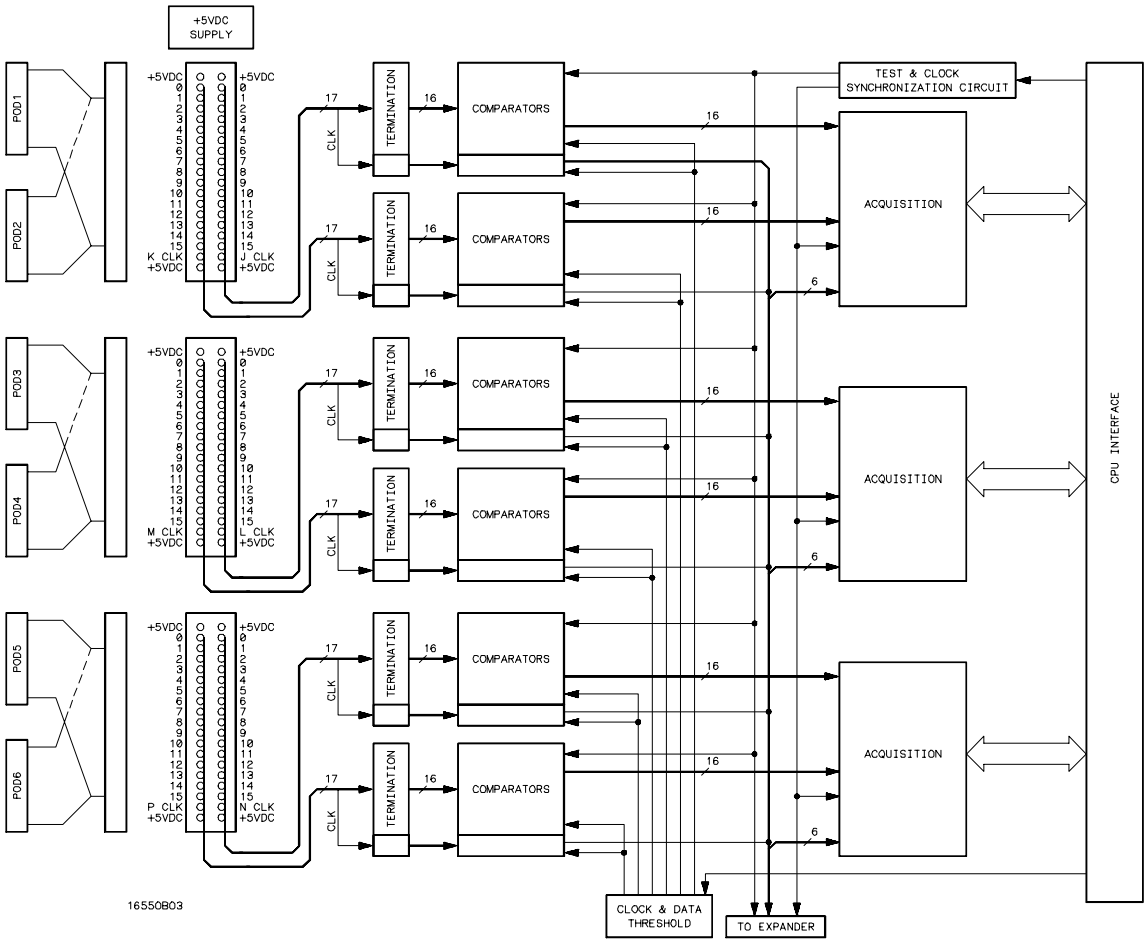
Theory of Operation

This chapter tells the theory of operation for the logic analyzer module and describes the self-tests. The information in this chapter is to help you understand how the module operates and what the self-tests are testing. This information is not intended for component-level repair.

Block-Level Theory

The block-level theory of operation is divided into two parts: theory for the logic analyzer used as a single-card module or as a master card in a multicard module, and theory for the logic analyzer used as an expander card in a multicard module. A block diagram is shown before each theory.

The HP 16550A logic analyzer



Probing The probing circuit includes the probe cable and terminations. The probe cable consists of two 17-channel pods that are connected to the circuit board using a high-density connector. For each pod, sixteen single-ended data channels and one single-ended clock/data channel are passed to the circuit board. If the clock/data channel is not used as a state clock in state acquisition mode, it is available as a data channel. The clock/data channel is also available as a data channel in the timing acquisition modes. The six clock/data channels plus the 96 data channels on each logic analyzer card results in a maximum of 102 available data acquisition channels for each card.

The pods include one ground path per channel in addition to a pod ground. The channel grounds are configured so that their electrical distance is the same as the electrical distance of the channel.

The probe tip assemblies and the terminations connected at the end of the probe cables have a divide-by-10 RC network that reduces the amplitude of the data signals as seen by the circuit board. This adds flexibility to the types of signals the circuit board can read in addition to improving signal integrity.

The terminations on the circuit board are resistive terminations that reduce transmission line effects on the cable. The terminations also improve signal integrity to the comparators by matching the impedance of the probe cable channels to the impedance of the signal paths of the circuit board. All 17 channels of each pod are terminated in the same way. The signals are still reduced by a factor of 10.

Comparators Two 9-channel comparators interpret the incoming data and clock signals as either high or low, depending on where the user-programmable threshold is set. The threshold voltage of each pod is individually programmed, and the voltage selected applies to the clock channel as well as the data channels of each pod.

Each of the comparators has a serial test input port used for testing purposes. A test bit pattern is sent from the Test and Clock Synchronization Circuit to the comparators. The comparators then propagate the test signal on each of the nine channels of the comparator. Consequently, the operating system software can test all data and clock channel pipelines on the circuit board through the comparator.

Acquisition Each acquisition circuit is made up of a single acquisition IC. Each acquisition IC is a 34-channel state/timing logic analyzer. Three acquisition ICs are included on every logic analyzer card for a total of 96 data channels and 6 clock/data channels. All of the sequencing, storage qualification, pattern/range recognition and event counting functions are performed by the acquisition IC.

Also, the acquisition ICs perform master clocking functions. All six state acquisition clocks are sent to each acquisition IC, and the acquisition ICs generate their own sample clocks. Every time the user selects RUN, the acquisition ICs individually perform a clock optimization before data is stored.

Clock optimization involves using programmable delays in the acquisition ICs to position the master clock transition where valid data is captured. This procedure greatly reduces the effects of channel-to-channel skew and other propagation delays.

In the timing acquisition mode, an oscillator-driven clock circuit provides a four-phase 125-MHz clock signal to each of the acquisition ICs. For high speed timing acquisition (125 MHz and faster), the four-phase 125-MHz clock signal determines the sample period. For slower sample rates, one of the three acquisition ICs divides the 125-MHz clock signal to the appropriate sample rate. The sample clock is then sent to the other two acquisition ICs.

Test and Clock Synchronization Circuit ECLinPS (ECL in pico seconds) ICs are used in the Test and Clock Synchronization Circuit for reliability and low channel-to-channel skew. Test patterns are generated and sent to the comparators during software operation verification (self-tests). The test patterns are propagated across all data and clock channels and read by the acquisition ICs to verify that the data and clock pipelines are operating correctly.

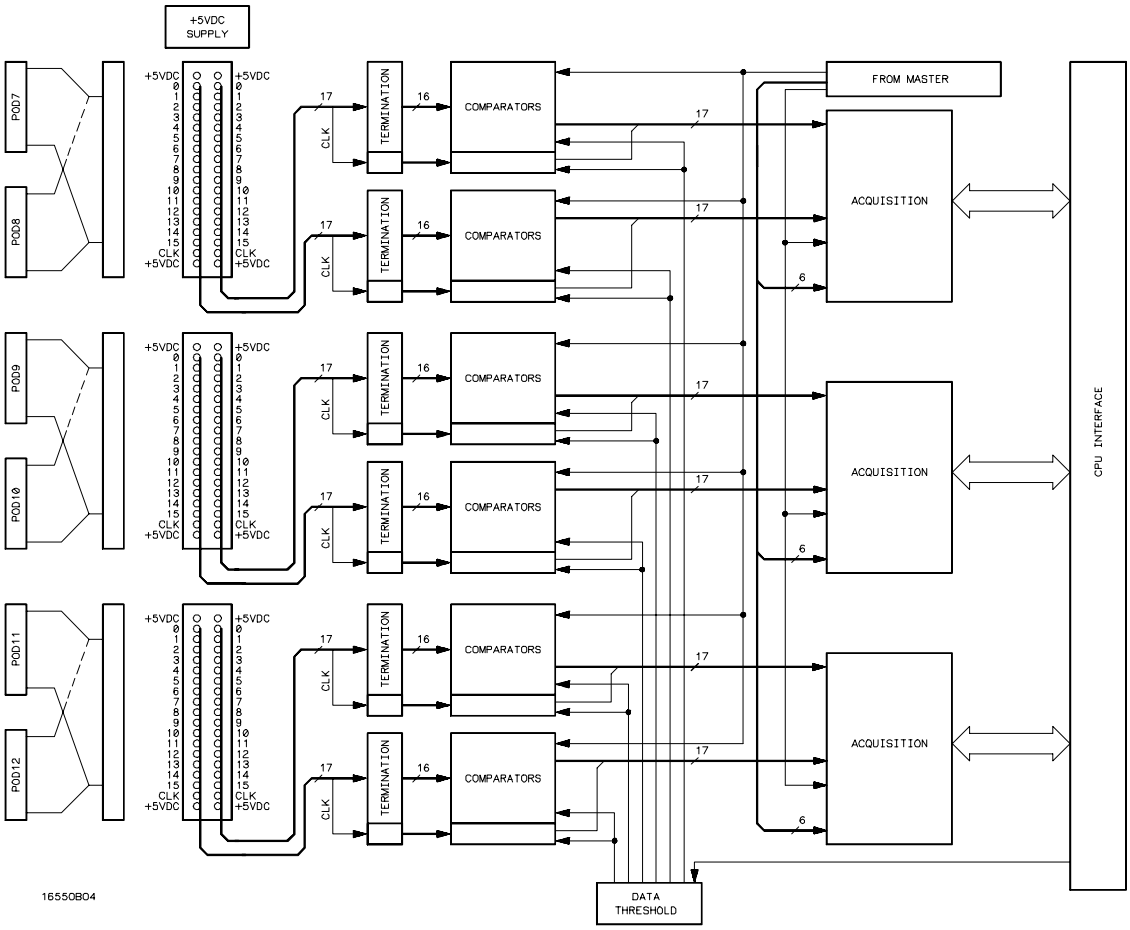
Also, the Test and Clock Synchronization Circuit generates a four-phase 125-MHz sample/synchronization signal for the acquisition ICs operating in the timing acquisition mode. At fast sample rates, the synchronizing signal keeps the internal clocking of the individual acquisition ICs locked in step with the other acquisition ICs in the module. At slower sample rates, one of the acquisition ICs divides the 125-MHz clock signal to the appropriate sample rate. The slow speed sample clock is then used by all three acquisition ICs.

Clock and Data Threshold The threshold circuit includes a precision octal DAC and precision op amp drivers. Each of the eight channels of the DAC is individually programmable which allows the user to set the thresholds of the individual pods. The 16 data channels and the clock/data channel of each pod are all set to the same threshold voltage.

CPU Interface The CPU interface is a programmable logic device that converts the bus signals generated by the microprocessor on the HP 16500A mainframe CPU card into control signals for the logic analyzer card. All functions of the state and timing card can be controlled from the backplane of the mainframe system including storage qualification, sequencing, assigning clocks and qualifiers, RUN and STOP, and thresholds. Data transfer between the logic analyzer card and the mainframe CPU card is also accomplished through the CPU interface.

+5 VDC supply The +5 VDC supply circuit supplies power to active logic analyzer accessories such as preprocessors. Thermistors on the +5 VDC supply lines and on the ground return line protect the logic analyzer and the active accessory from overcurrent conditions. When an overcurrent condition is sensed, the thermistors create an open that shuts off the current from the +5 VDC supply. After a reset time of approximately 1 minute, the thermistor closes the circuit and makes the supply current available.

The HP 16550A logic analyzer as an expander



Two HP 16550A logic analyzers can be connected together in a two-card master/expander configuration. All of the functions of the logic analyzer configured as a master are retained by the logic analyzer configured as an expander with a few exceptions. As a master and expander two-card logic analyzer module, most of the supporting circuitry on the expander configured card is disabled to allow both the master and expander cards to operate together as one 204-channel module with no compromise in functionality. The same signals that drive the acquisition ICs on the master configured card also drive the acquisition ICs on the expander configured card.

Acquisition The six clocks sent to the master card are also sent to the acquisition ICs on the expander card. The acquisition ICs on the expander card individually generate their own master clock for the state acquisition mode. For timing acquisition mode, the master card also passes the synchronization signal to the expander card.

The six clock/data lines on the expander card pods are not available for either state mode clocking or state clock qualification. However, the six clock/data lines are still available as data channels.

Test and Clock Synchronization Circuit The signals generated by the Test and Clock Synchronization Circuit of the master card are sent to the expander card. Consequently, the Test and Clock Synchronization Circuit on the expander card is disabled to allow the master configured card to drive the expander configured card. The functionality of the Test and Clock Synchronization Circuit remains the same, but the circuit drives three more acquisition Acquisition IC and six more comparator test inputs.

Threshold The thresholds of each of the expander card pods are individually programmable, as with the master card pods. The threshold of the data and clock/data channels of each pod is set to the same threshold voltage. The clock/data channel on each pod of the expander card is available only as a data channel.

Self-Tests Description

The self-tests for the logic analyzer identify the correct operation of major functional areas in the module. There are three types of self-tests: the Board Test, the Chip Tests, and the Data Input Inspection. The self-tests are not intended for component-level diagnostics.

Board Test

The Board Test functionally verifies the two oscillators and the twelve 9-channel comparators on the circuit board. First, the oscillators are checked using the event counter on one of the acquisition ICs. The event counter will count the number of oscillator periods within a pre-determined time window. The count of oscillator periods is then compared with a known value.

The comparators are then checked by varying the threshold voltage and reading the state of the activity indicators. The outputs of the octal DAC are set to the upper voltage limit and the activity indicators for all of the pod channels are read to see if they are all in a low state.

The octal DAC outputs are then set to the lower voltage limit, and the activity indicators are read to see if they are in a high state. The DAC outputs are then set to 0.0 V, allowing the comparators to recognize the test signal being routed to the test input pin of all of the comparators. Consequently, the activity indicators are read to see if they show activity on all channels of all of the pods.

Chip Tests

During the Chip Tests, six tests are performed on the acquisition ICs. The tests are the Communications, Memory, Encoder, Resource, Sequencer, and Clock Generation Tests.

Communications Test The communications test verifies that communications pipeline between the various subsystems of the IC are operating. Checkerboard patterns of "1s" and "0s" are routed to the address and data busses and to the read/write registers of each chip. After verifying the communications pipelines, the acquisition clock synchronization signals that are routed from IC to IC are checked. Finally, the IC master clock optimization path is checked and verified.

Passing the communications test implies that the communications pipelines running from subsystem to subsystem on the acquisition IC are functioning and that the clock optimization circuit on the IC is functioning. Also, passing this test implies that the acquisition clock synchronization signals are functioning and appear at the synchronization signal output pins of the acquisition IC.

Memory Test Acquisition RAM is checked by filling the IC RAM with a checkerboard pattern of "1s" and "0s," then reading each memory location and comparing the test pattern with known values. Then, the IC RAM is filled with an inverse checkerboard pattern, read, and compared with known values.

Passing the memory test implies that the acquisition IC RAM is functioning and that each memory location bit can hold either a logic "1" or logic "0."

Encoder Test The encoder in the FISO front end is tested and verified using a walking "1" and walking "0" pattern. The walking "1" and "0" is used to stimulate all of the encoder output pins which connect directly to the FISO memory cells. Additionally, the post-store counter in each of the acquisition ICs is tested.

Passing the encoder test implies that the FISO encoder is functioning and can properly route the acquired data to the acquisition memory FISO RAM. Also, passing this test implies that the post-store counter on the acquisition ICs is functioning.

Resource Test The pattern, range, edge, and glitch recognizers are tested and verified. First, the test register is verified for correct operation. Next, the pattern comparators are tested to ensure that each bit in the recognizer memory location as well as the logic driver/receiver are operating. The edge and glitch pattern detectors are then verified in a similar manner. The range detectors are verified with their combinational logic to ensure that the in- and out-of-range conditions are recognized.

Passing the resource test implies that all of the pattern, range, edge, and glitch resources are operating and that an occurrence of the pattern, edge, or glitch of interest is recognized. Also, passing this test implies that the range recognizers will detect and report in- and out-of-range acquisition data to the sequencer or storage qualifier. The drivers and receivers at the recognizer input and output pins of the acquisition IC are also checked to be sure they are functioning.

Sequencer Test The sequencer, the state machine that controls acquisition storage, tested by first verifying that all of the sequencer registers are operating. After the registers are checked, the combinational logic of the storage qualification is verified. Then, both the occurrence counter and the sequencer level counter is checked.

Passing the sequencer test implies that all 12 available sequence levels are functioning and that all possible sequence level jumps can occur. Also, passing this test implies that user-defined ANDing and ORing of storage qualified data patterns will occur, and that the occurrence counter that appears at each sequence level is functioning.

Clock Generator Test The master clock generator on the acquisition ICs are tested by first checking the operation of the clock optimization circuit. The state acquisition clock paths are then checked to ensure that each state clock and clock qualifier are operating by themselves and in all possible clock and qualifier combinations. The timing acquisition optimization circuit is then operationally verified. Finally, the timing acquisition frequency divider (for slower timing sample rates) is checked.

Passing the clock generator test implies that each acquisition IC can generate its own master clock whether the clock is generated using a combination of external clocking signals (state mode) or internal sample clock signals (timing mode).

Data Input Inspection

The data input inspection allows a user to verify that all of the data and clock/data pipelines are operational. When the data input inspection test is selected, a test signal is fed to the test input pins of all twelve 9-channel comparators. The test menu displays the activity indicators for all data and clock/data channels, which should show transitioning data signals on all channels.

The data input inspection is not an active part of the performance verification. However, the test is useful for identifying failed channels in order to temporarily work around the problem until the logic analyzer module can be sent to an HP service center for repair.